Design Considerations for Wolfspeed Gen3 SiC MOSFET and 650V MOSFET Gate Driving Recommendations

August 2020

Clarification of V_{GS}

Max Gate Drive Voltage

Maximum Rating 650V MOSFET

V_{GS}	Gate - Source voltage (Under transient events < 100 ns)	-8/+19	V	Fig. 29

V_{GS} maximum rating is -8/19V as shown in the waveform. The positive max V_{GS} rating is 19V. The negative max V_{GS} rating is -8V. The max V_{GS} rating allows for ringing and overshoots that will be superimposed on top of the continuous gate drive voltage. As long as the peak transient voltages don't exceed the part's max V_{GS} rating, the device will run properly and there is no degradation to the device's life or reliability. For negative V_{GS} , the pulse width must be less than 100ns when Vgs <-6V in the transient events.

- Negative Gate-Source bias voltage will ensure MOSFET staying off for half bridge topology to avoid parasitic turn-on due to cross talk.
- +15V/-3V is recommended. The users can choose turn-off voltage range -2V~ -4V.

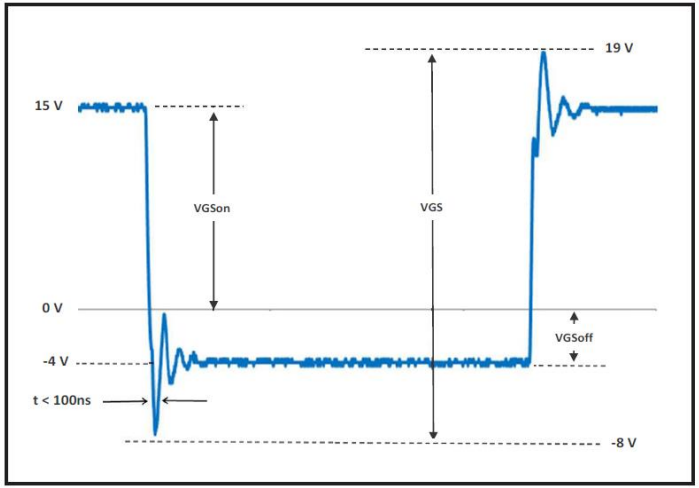
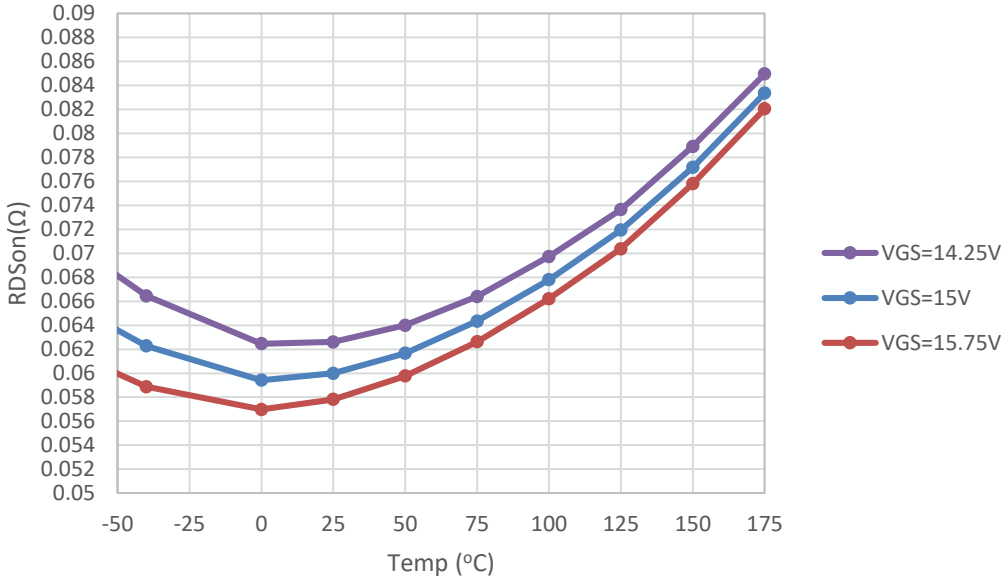


Fig. 29

Rdson under Turn-on Voltage Tolerance C3M0060065K testing



In practical design, power supply tolerance must be considered. The guidance is within +/-5% tolerance.

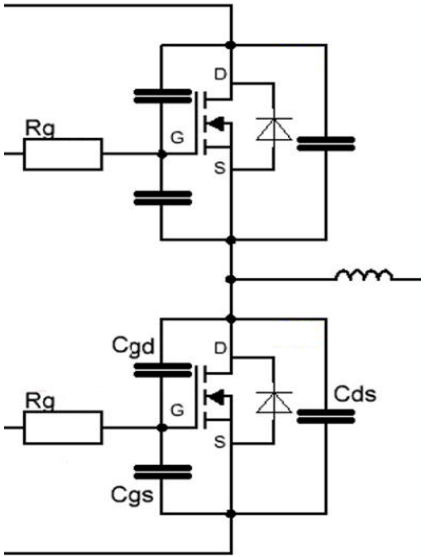
The impact of Rdson due to V_{GS} variation. Rule of thumb, the 5% of gate voltage tolerance will cause around 4% Rdson variation at 25°C and 2% variation at 125 °C.

Why Negative Voltage Is Required in Half Bridge?

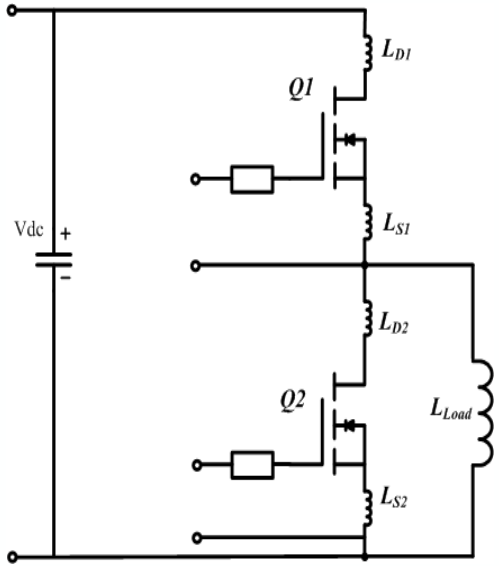
Why negative driving voltage?

If Gen3 MOSFET is fully turned off at 0V, then why it is recommended negative turn-off voltage?

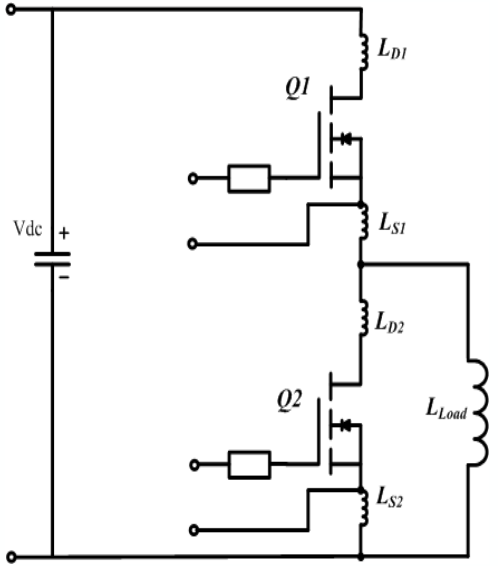
Cross Talk in Totem Pole Half Bridge (Totem Pole)



Ideal Switch without package parasitic

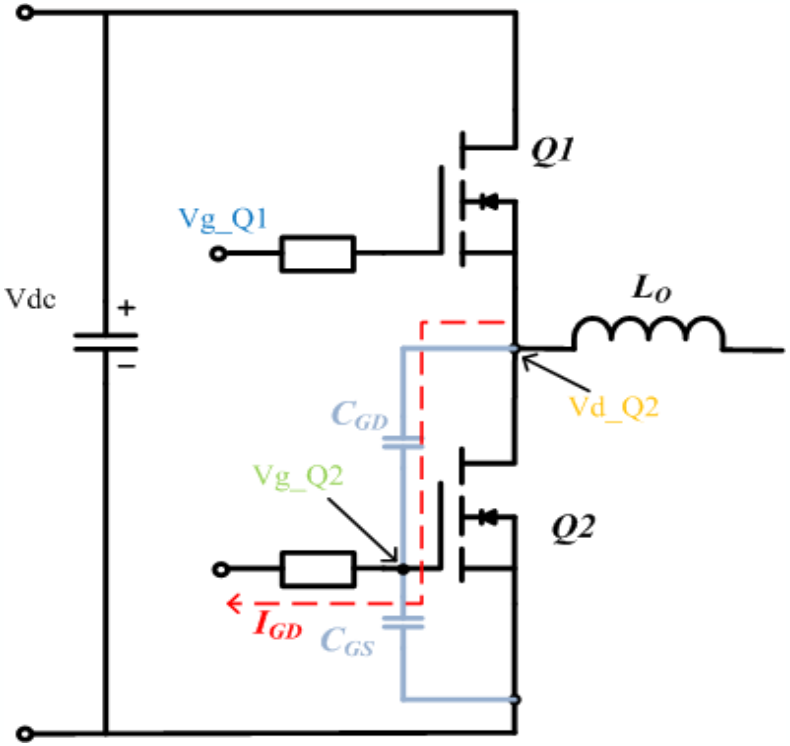


3L package

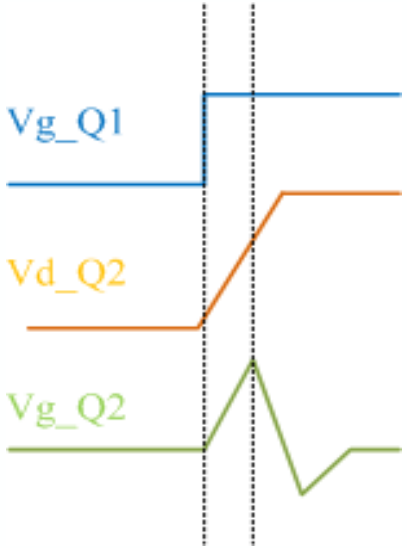


4L package

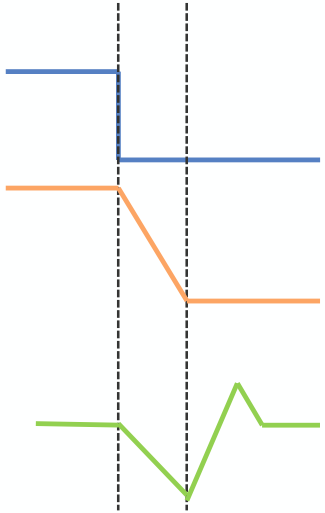
Cross Talk in Ideal Totem Half Bridge by dv/dt Only



Turn on Q1



Turn off Q1



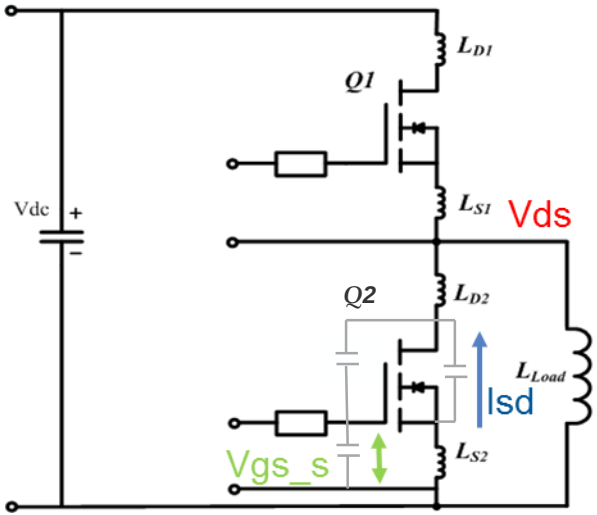
If dv/dt=100V/ns, and C_{GD}=10pF

I_{GD} ~ C_{GD} * dv/dt=1A

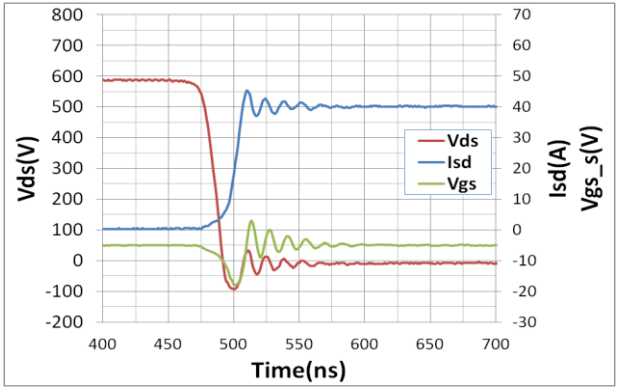
Vgs_spike ~ Rg* I_{GD}

Cross Talk in Non-ideal Totem Pole by dv/dt and di/dt

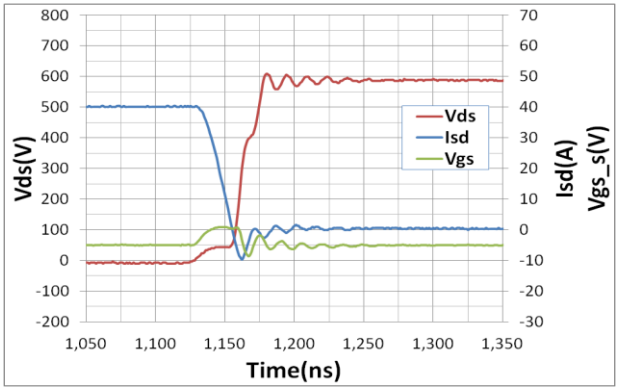
It is more complicated in real circuit due to parasitic inductance inside the device and in the circuit



Turn off Q1



Turn on Q1



Discussion on Totem Pole Half Bridge

Cross talk exists in Totem Pole half bridge topology

1. It depends on parasitic capacitance of devices and layout parasitic inductance
2. It depends on how fast the device switches

From the test result, the voltage spike on the gate caused by the cross talk during turn-on transition can be above 3V, which is above Gen3 MOSFET typical $V_{GS(th)}$.

The risk of using zero voltage in half bridge topology:

1. Increase switching loss
2. Potential shoot through

It is recommended to drive Wolfspeed Gen3 MOSFET +15V/-3V for Totem Pole half bridge topology. Negative gate bias voltage will guarantee the device stays off in all conditions.

Competitor Analysis: Trench MOSFET

Competitor

Gate-source threshold voltage	$V_{GS(th)}$	*(tested after 1 ms pulse at V_{GS}=+20 V)* I_D = 10mA, V_{DS} = V_{GS} T_j = 25°C T_j =175°C	3.5 -	4.5 3.6	5.7 -	V

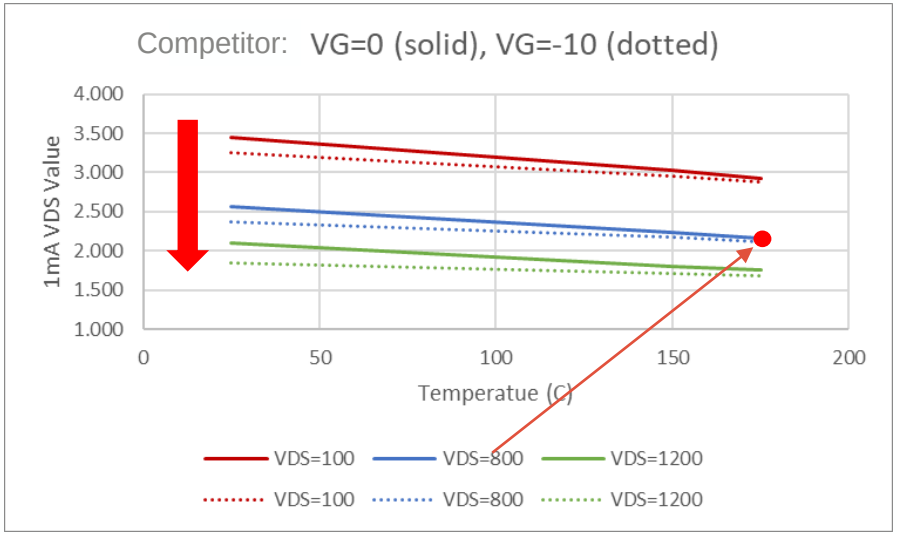
Wolfspeed

$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_D = 11.5 mA	Fig. 11
			2.0		V	V_{DS} = V_{GS}, I_D = 11.5 mA, T_J = 175ºC	

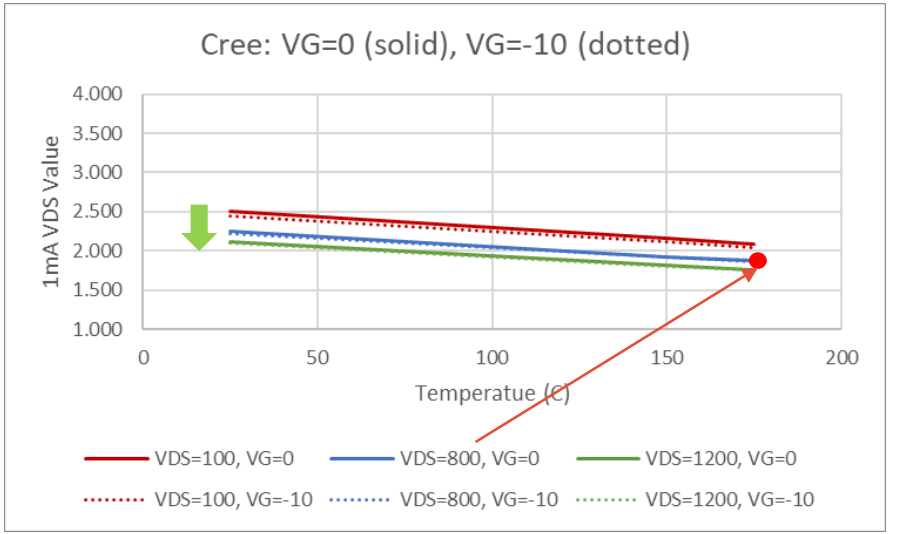
Competitor's $V_{GS(th)}$ is much higher than Wolfspeed Gen3 MOSFET under the data sheet condition. However, the test condition Vds=Vgs is not real application condition. Due to the trench structure, the $V_{GS(th)}$ in the high voltage switching condition is not as high as the value in the datasheet.

$V_{GS(th)}$ Measurement at High Voltage

Competitor's 45mO/1200V



Wolfspeed C3M0032120K



Trench MOSFET $V_{GS(th)}$ is reduced significantly at high Vds. In datasheet $V_{GS(th)}$ =4.5V is tested under condition Vds@20V. At Vds 800V (a typical working voltage of the device) and 25ºC , $V_{GS(th)}$ of the trench device falls to 2.5V, reduction by 45%, and $V_{GS(th)}$ of the Wolfspeed device only falls by 10%.
At 175ºC, $V_{GS(th)}$ of the trench device is further reduced to 2.2V.

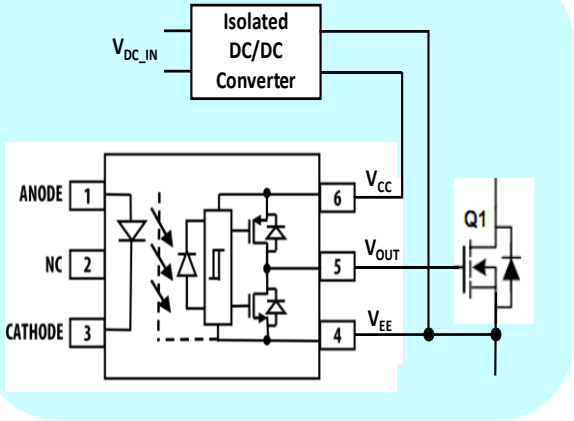
Summary on Negative Gate Voltage for Half Bridge

Drive Wolfspeed Gen3 MOSFET with gate voltage +15V/-3V for Totem Pole half bridge topology. Negative gate bias voltage will guarantee the device stays off in all conditions.

Gate Driver and Bias Power Supply

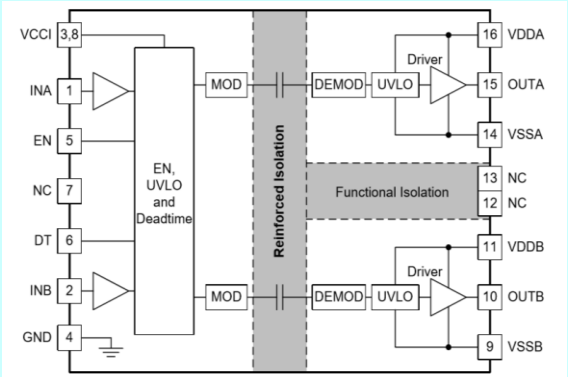
Types of Isolated Gate Driver

Optically Isolated



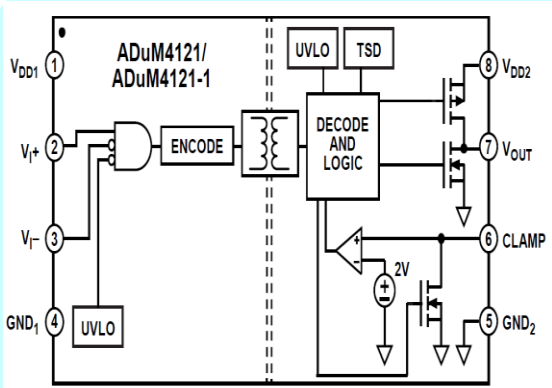
Broadcom

Capacitive Isolated



TI, Silicon Labs

Inductive Isolated



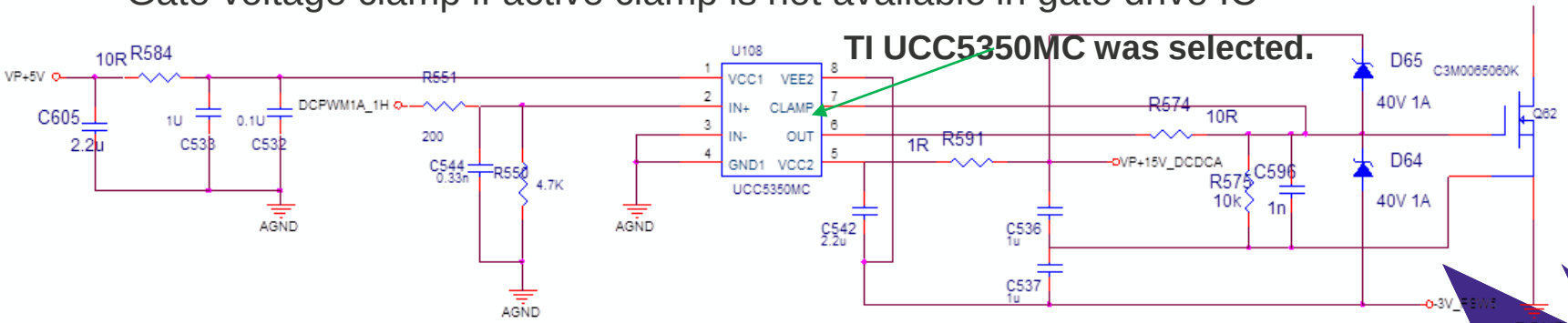
ADI, NXP

Quick Summary of Pros and Cons of different types of GD Technology

- Capacitive: very fast, small propagation delay, concern in high electrical field application
- Inductive: mature technology, concern in high magnetic field application
- Optical: large physical distance, good for high isolation voltage, but there is photo gain deterioration over time concern

Tips for SiC MOSFET Gate Driver Circuit

- CMTI (>100KV/us)
- VIORM Maximum Working Insulation Voltage
- Driving capability
- Propagation delay time (~50nS) and channel mismatch time (~10nS)
- Active miller clamp
- Gate supply voltage (+15V/-3V)
- Additional cap or RC from Gate to Kelvin Source
- Gate voltage clamp if active clamp is not available in gate drive IC

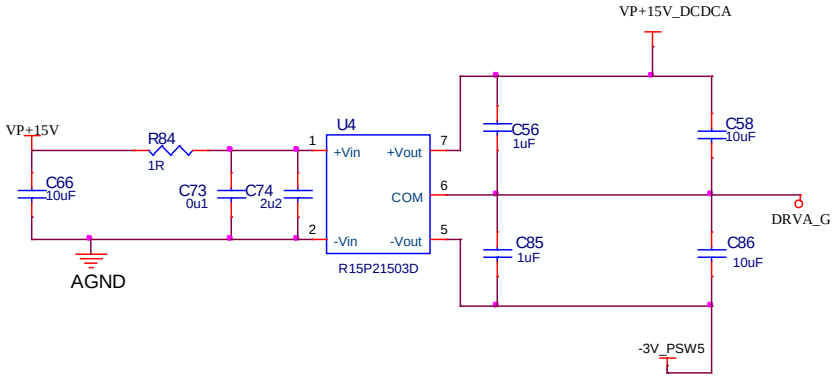


How to Generate Negative Voltage? Option 1

Dedicated +15V/-3V power supply

Wolfspeed has worked with partners (RECOM, MOURSUN) to make power modules

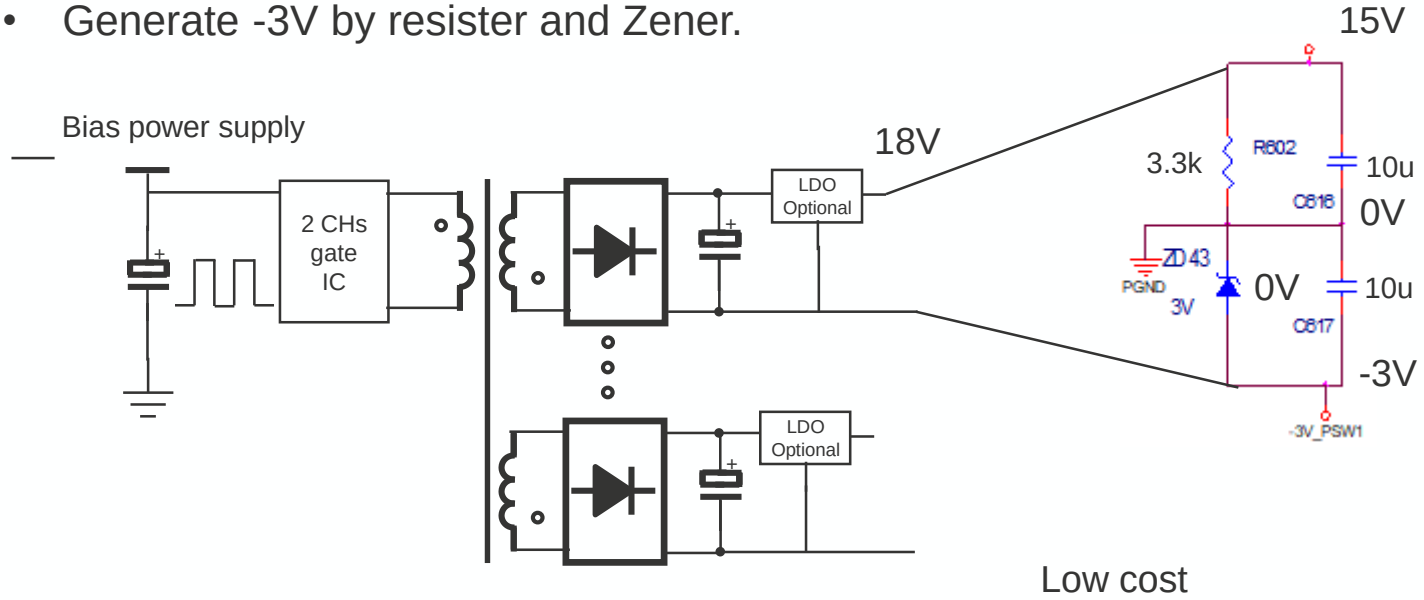
- RECOM R15P21503D and R12P21503D
- MOURSUN QA15115R2



Easy to use

How to Generate Negative Voltage? Option 2

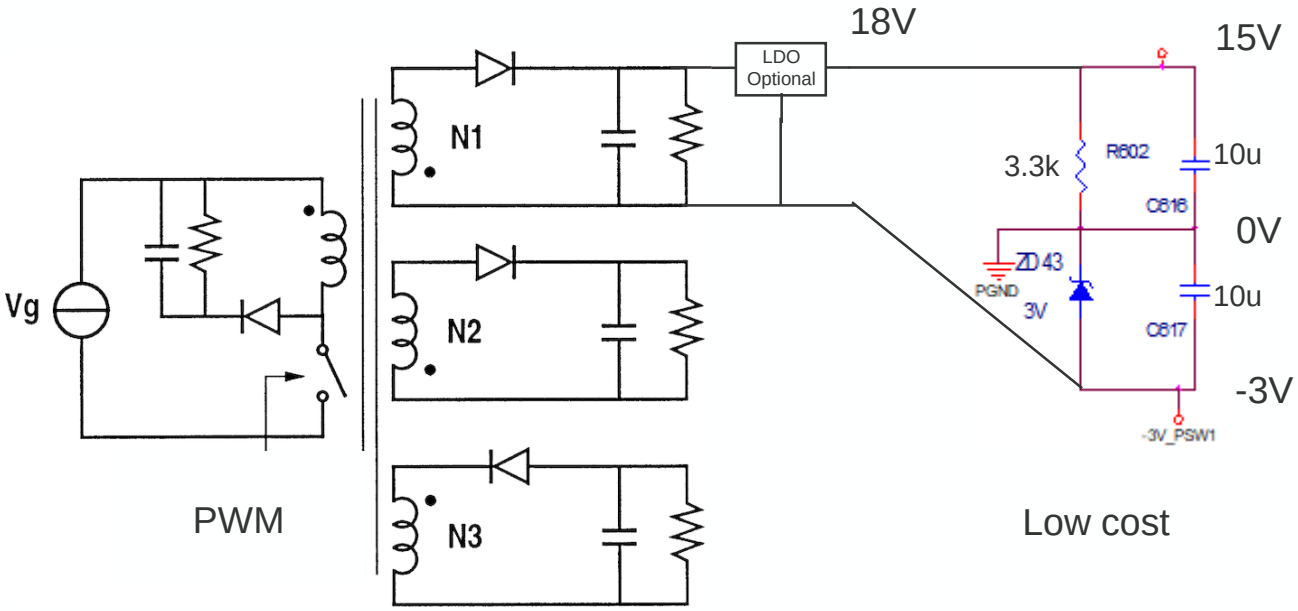
- Open loop controlled 18V multi-outputs Aux power supply based on bias power supply of the system.
- Generate -3V by resister and Zener.



Low cost

How to Generate Negative Voltage? Option 3

- Closed loop controlled 18V multi-outputs flyback converter.
- Generate -3V by resister and Zener.



Design and Control Mistakes

“You Can’t Get The Expected Performance From a Bad Design, Even You Are Using The Best Components”

Design and Control Mistakes

- Wrong Gate Drive Voltage
- Over-Voltages
- Over-Currents
- Over-Temperature
- Unstable Bias Supply for Gate Drive
- Poor Gate Drive Circuit
- Unsuitable Thermal management
- Unsuitable Switching Frequency Selection
- Unsuitable Mechanical Design

Wrong Gate Voltage

Popular wrong gate voltage cases

1. Transferring from Wolfspeed Gen2 to Gen3
2. Transferring from Si to SiC
3. Transferring from 18V SiC to Wolfspeed Gen 3

Wolfspeed Gen3 MOSFET				
Steady Vgs+	+20V	+12V	+18V	+15V
Steady Vgs-	-5V	0V	-2V	-3V（-4V）

Wolfspeed Gen2

Si MOSFET

Rohm
Infineon
ST

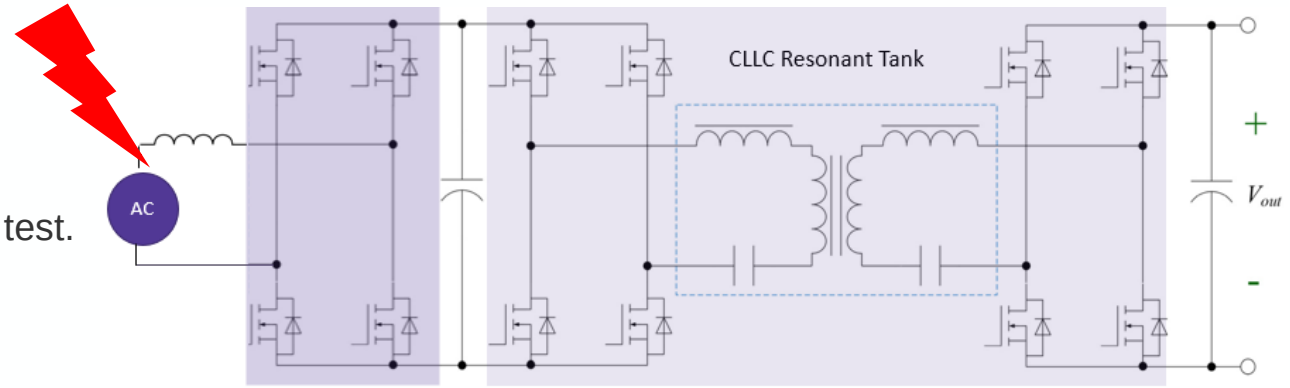
Wolfspeed Gen3
ON 900V
AOS 1200V
Ifx 1200V 45mohm
ST Gen3(coming)
Rohm Gen4(coming)

Electrical Over Stress(EOS)

Voltage and current stress are evaluated at normal conditions.

But it is over stress in transient events or EMC test. Higher dV/dt ad di/dt will cause higher voltage spike. Surge current and voltage should be evaluated.

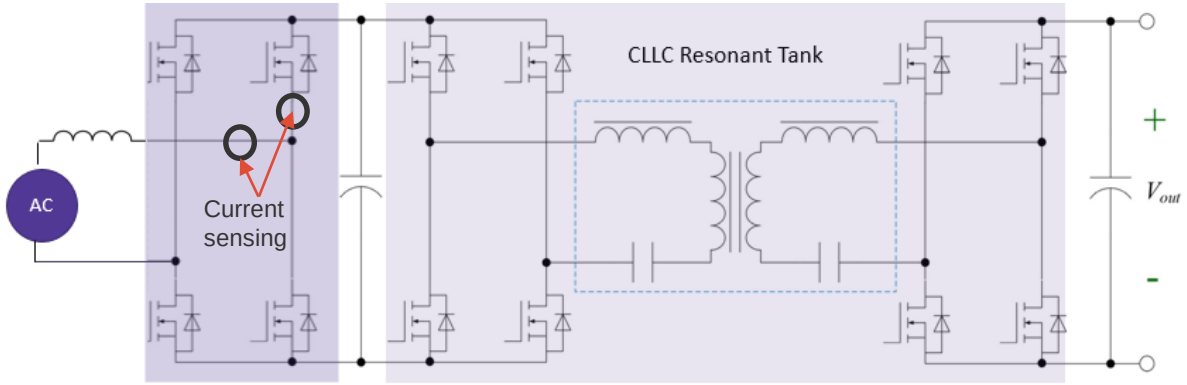
1. Step load
2. Input Transient
3. Short circuit
4. Surge/lightning test.
5. ESD test



Solution:

Suggest customers to complete the evaluation in design stages as early as possible.

Wrong Cycle by Cycle Current Limit

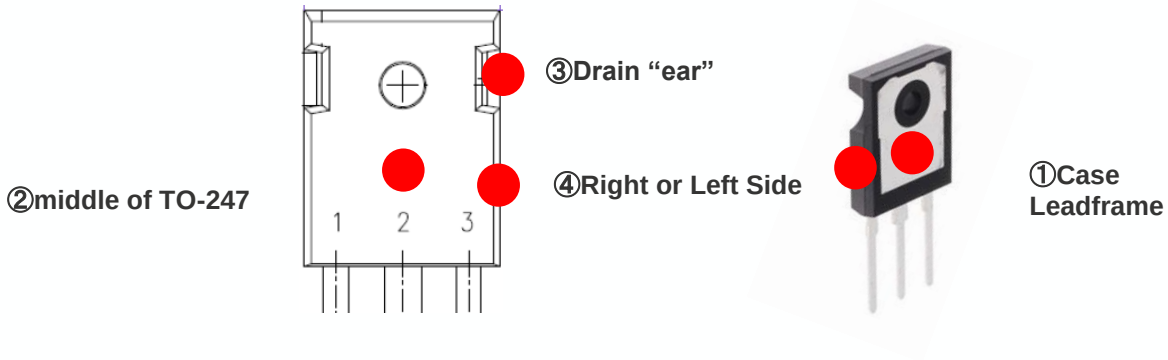


1. Power magnetics should not be saturated at the CBC limit
2. Current transformer(if it is used) should not be saturated at the CBC limit
3. The output of current sensing should not exceed Vdd of DSP
4. The selected power components should not over current stress at CBC limit
5. The converter should provide the required output power during CBC mode

Thermal Over Stress

Popular mistakes

1. Use measured case temperature as junction temperature.
2. Wrong measurement in thermal test
3. Thermal test is only done at steady condition(low input & full load). And there is no enough margin. Thermal over stress happens in an OTP event.
4. Thermal is not evaluated in pulse load operation mode



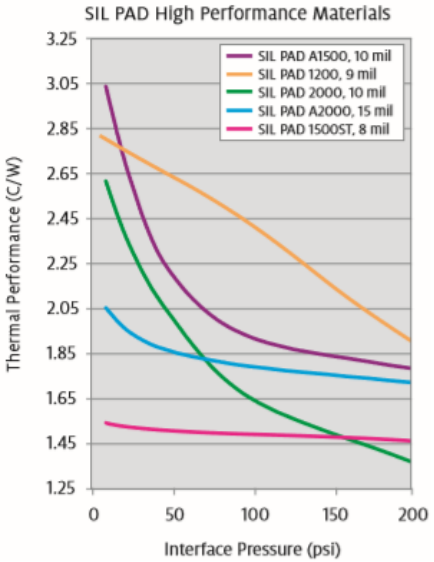
Unsuitable Thermal Management

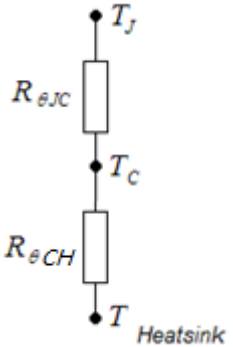
It is a very important topic for SiC. With a smaller die, SiC device has larger Rth_jc.

Without a proper thermal management, the overall cost of the system becomes high.

Common Mistakes:

1. T_heatsink is too high in the design. for example, 110degC.
2. Low cost TIM makes the system not cost-effective. High thermal resistance TIM is not saving but wasting your BOM cost.

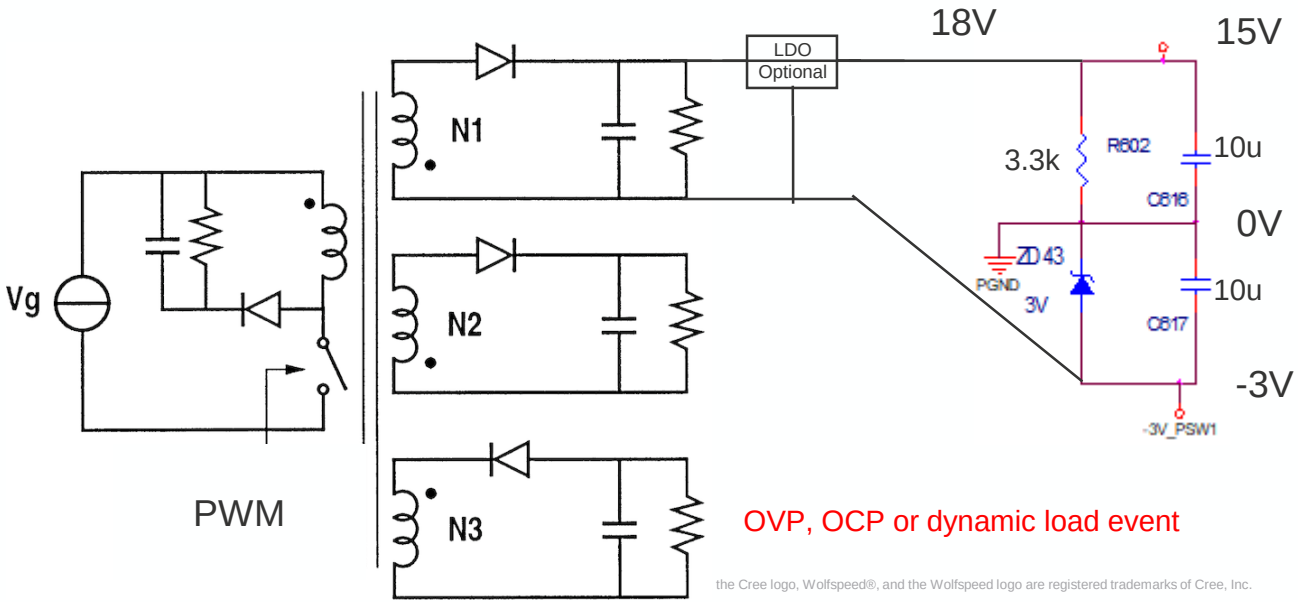




Unstable Bias Suppliers for Gate driver

The same Aux power supply provides both the internal bias supplies and the standby output of the units.

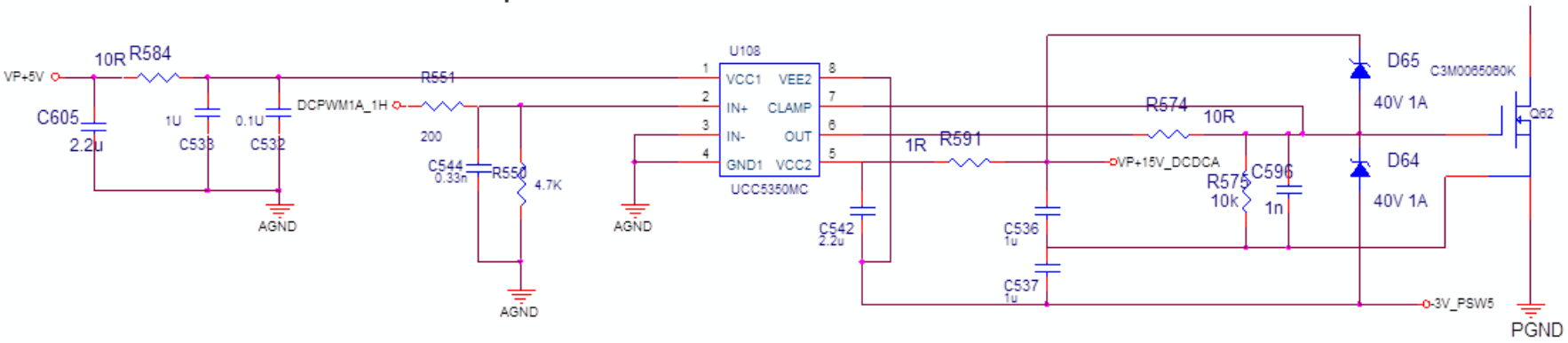
Issue happens during standby output OVP, OCP or dynamic load event.



Wrong Gate Driver IC

Wrong rated gate drive IC

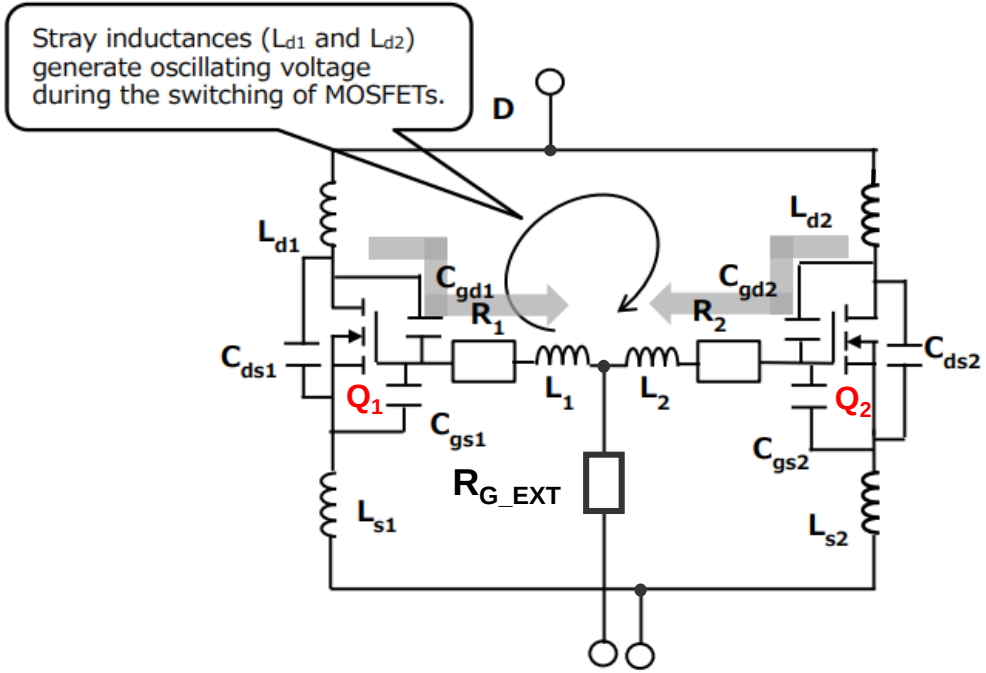
- Insufficient Working Insulation Voltage
- Insufficient driving current capability
- Insufficient CMTI
- Long propagation delay or large tolerance
- No active miller clamp

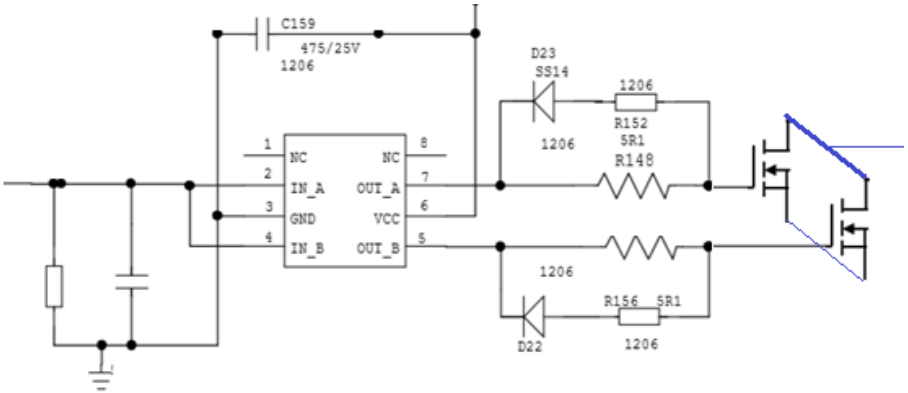


Examples: Good gate drivers for SiC from TI (UCC5350MC), ADI(ADuM4121), SiLabs (Si823HX)

Wrong Gate Drive Circuit in paralleling MOSFETs

1. Common external gate resister to drive MOSFETs in parallel
2. Different gate drivers to drive MOSFETs in parallel

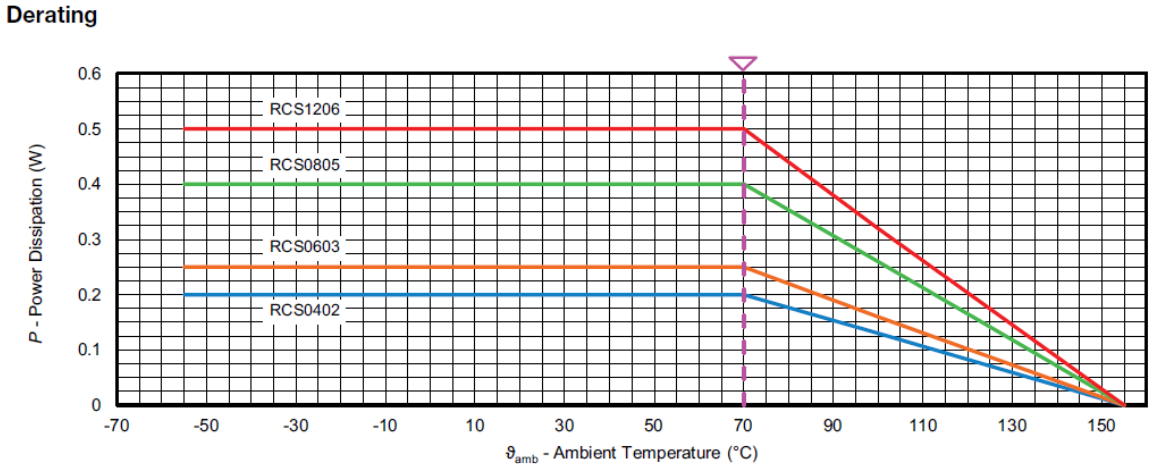




Recommendation: Same gate driver with separated external gate resistors.

Wrong Power rating for Gate Resistor

Some customers just use 0805 or 1206 resistors for all applications.



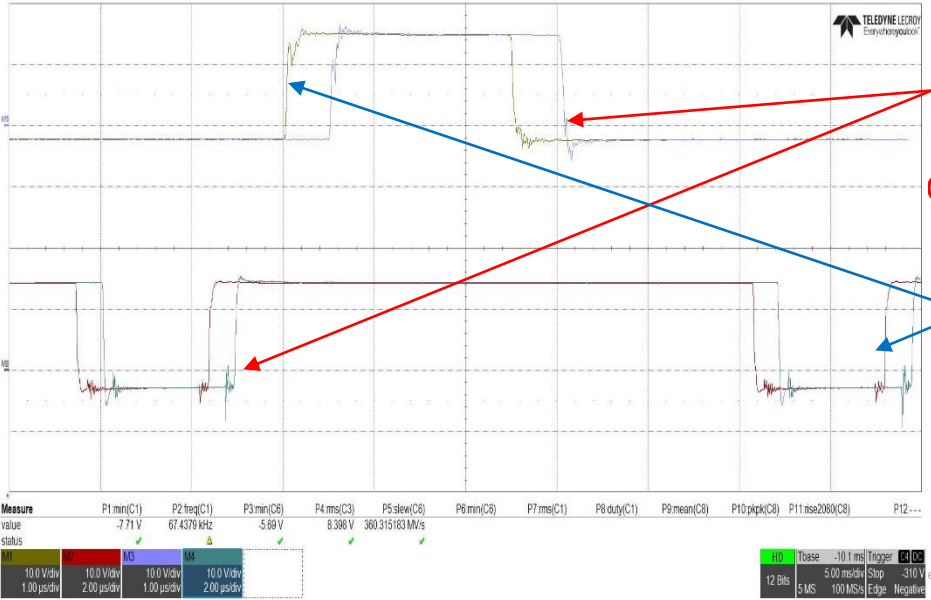
Tips:

- ✓ Select gate resistors with proper power rating. (Qg, f_sw, ambient temperature)
- ✓ Consider power derating in gate resistors selection based on actual temperature
- ✓ Resistor with surge pulse capability is preferred

Wrong Gate Bead Placement

A small capacitor (typical from 100pF to 1nF) between the gate and source of MOSFET. This capacitor provides a low impedance path for high frequency noise currents to bypass the gate. A wrong gate bead placement(on the lead) will disable the low impedance path.

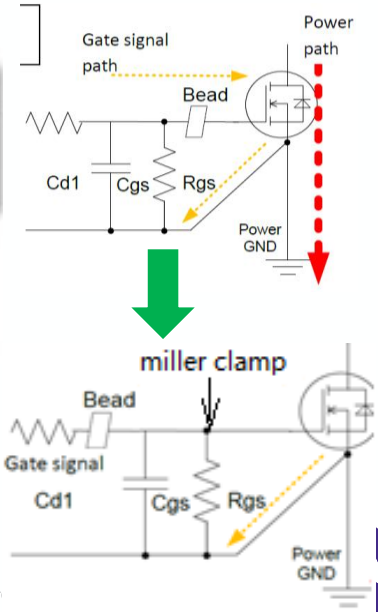
You will get a better waveform at the solder joint or lead end. However, the actual ringing or voltage spike can be much worse at the root of the device. You just have a LC filter…



Test point 1:
At root of the device

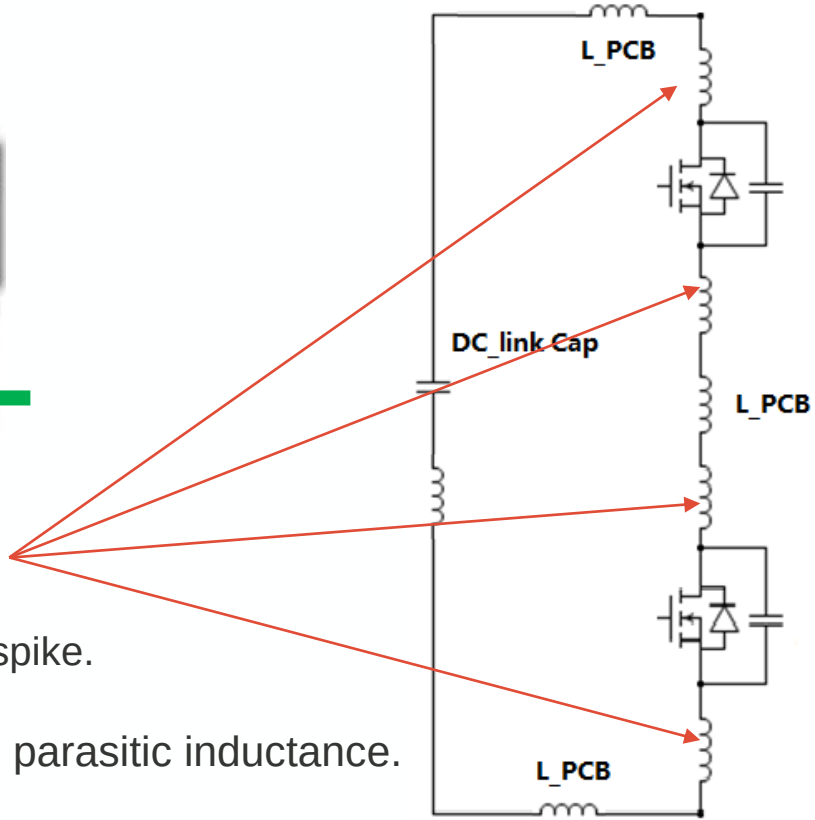
On-device gate bead

Test point 2:
Solder joint or lead



Voltage Spike due to Long Lead

or



L =0.2*10*(Ln(2*10/5)+0.2235*1/10+0.5)=5.7nH

ΔV=L*di/dt= 5.7*2*50/20=29V additional voltage spike.

- Long lead introduces drain voltage spike due to parasitic inductance.
- Long lead introduces gate voltage oscillation.

Unsuitable Switching Frequency

Mistakes on Switching Frequency Selection:

1. Too high switching frequency for high voltage hard switching applications
2. Non-EMI-friendly switching frequency

Good switching frequency range for high voltage hard switching applications

- <=47kHz
- 60~67kHz
- 120~135kHz

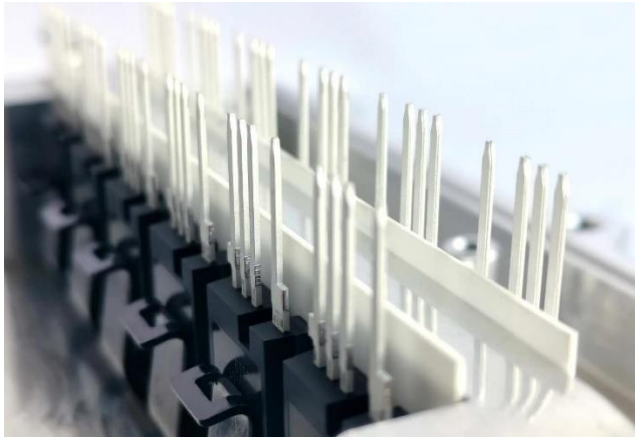
Insufficient Isolation

Insufficient Isolation between the power components and heatsink.

Enough clearance and creepage are required. Not only from drain pad but also the leads to heatsink.

For high voltage application, for example 800V DC link

TIM should cover both the body and leads to keep >=4mm(TBD based on different standard and applications)



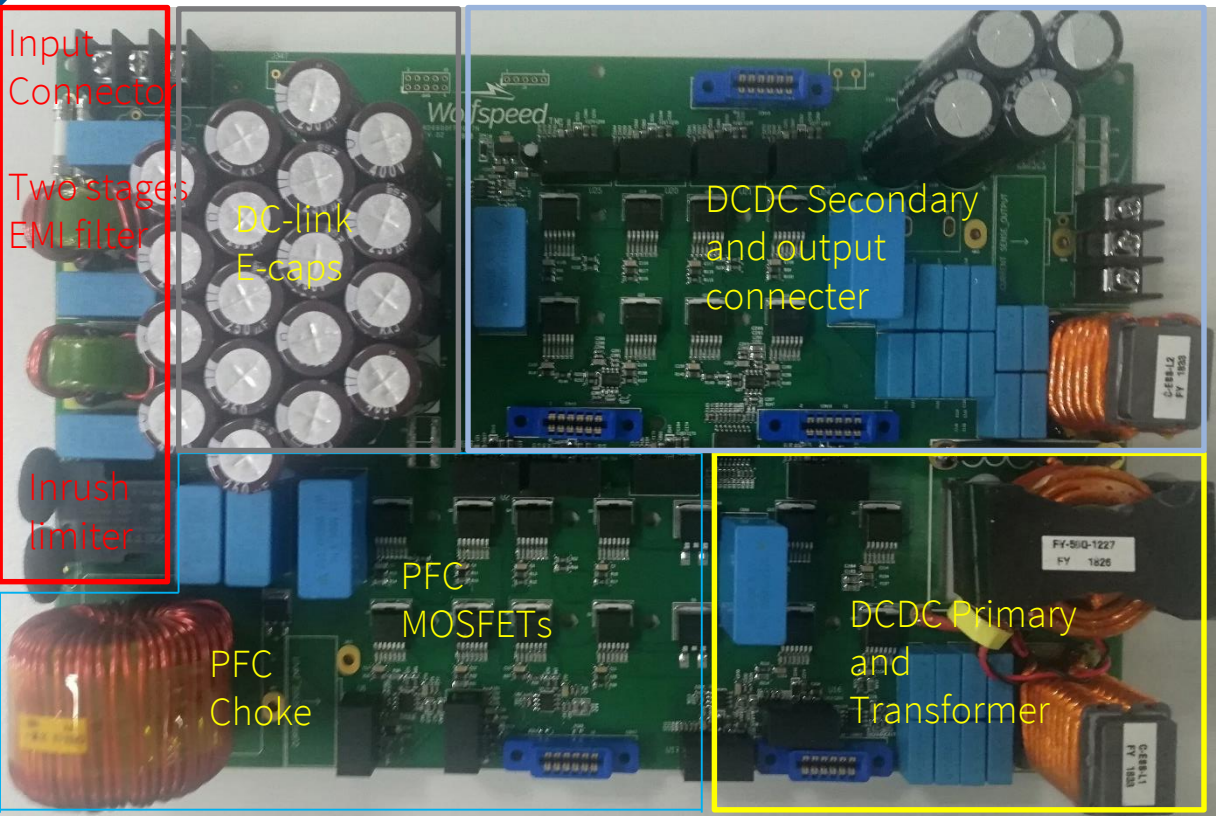
PCB Layout Mistakes

“YOU CAN’T RECOVER FROM A BAD LAYOUT”

PCB Layout Mistakes

- Poor Components Placement
- Poor Multi-layer PCB Design
- Large Commutation Loop
- Large Area for high dV/dt node
- Insufficient Creepage/clearance
- Gate and Drain Overlap
- Long Distance Between Gate Driver and MOSFET
- Poor Layout for Sensitive Networks
- Poor Layout for MOSFETs in Parallel

Poor Components Placement



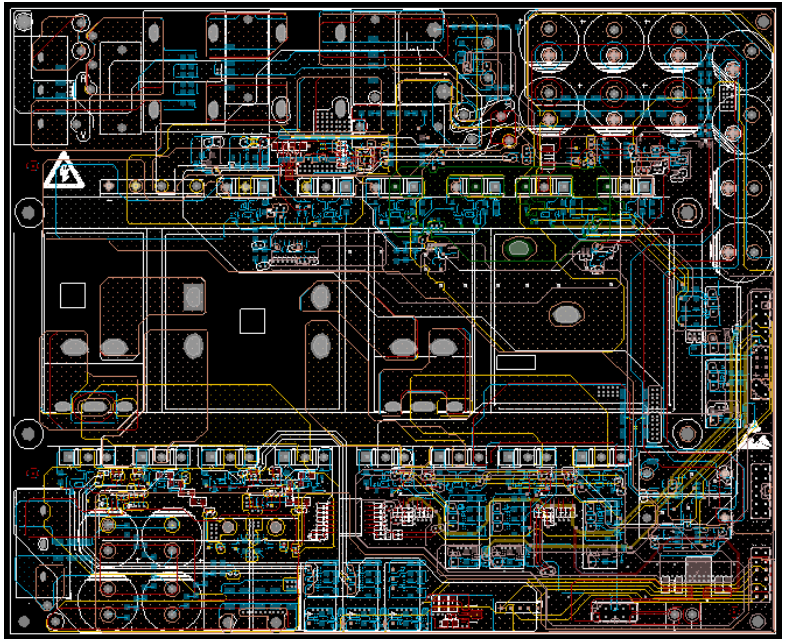
Common Mistakes:

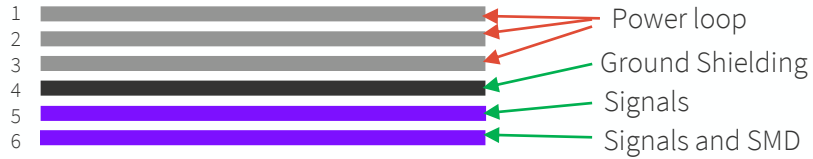
Place power magnetics or MOSFETs Nearby input/output connector. This will cause EMI issues.

Tips:

- Keep the high dV/dt trace/nodes far away from the input EMI filter and connector to minimize the noise coupling.
- Keep the high magnetic field such as PFC choke, DCDC power magnetics far away from the input EMI filter and connector to minimize the noise coupling.

6 layers Power Board

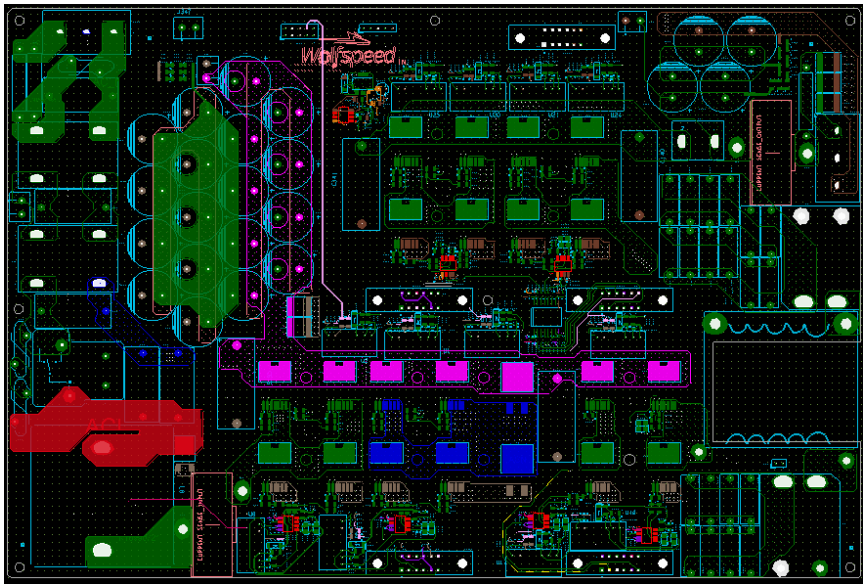


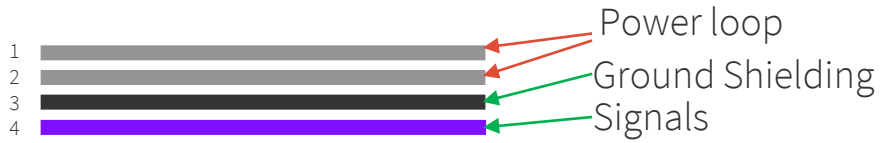


Tips(for 6layers PCB):

- 1st , 2nd and 3rd layers for power loop
- 4th layer for GND. The ground layer acts as a shielding to cover the signal traces at bottom layer.
- Sensitive signals at 5th layer
- Sensitive signals and SMD at 6th layer

4layers Power Board



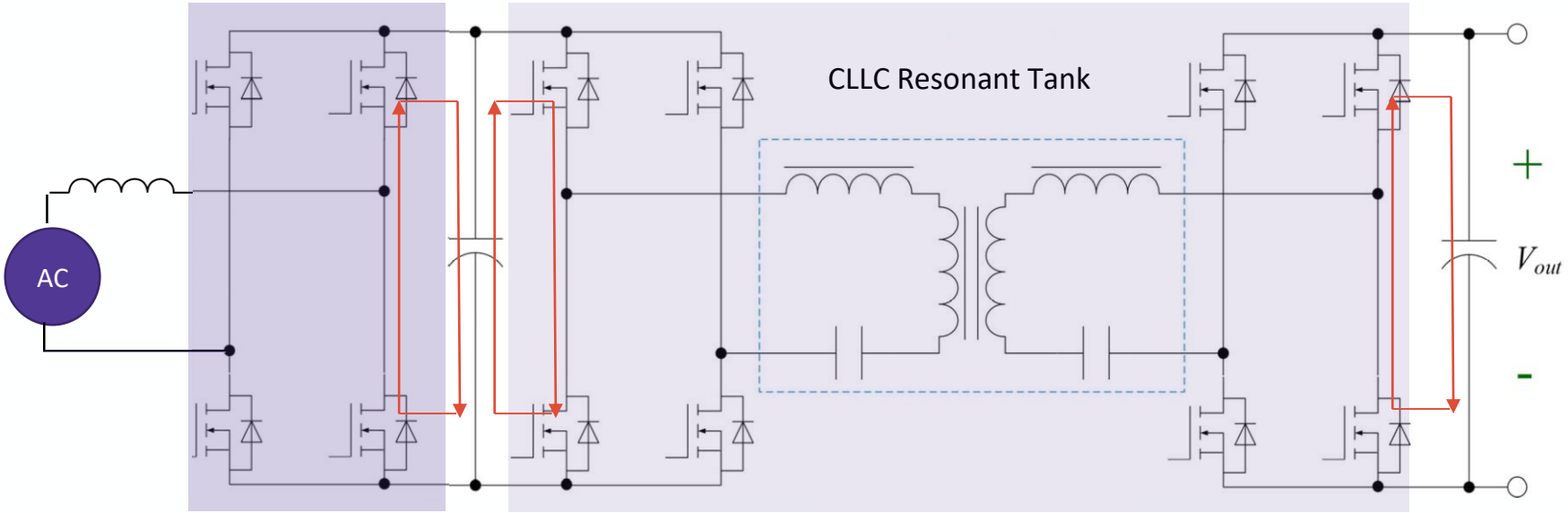


Tips(for 4layers PCB):

- 1st and 2nd layers for power loop
- Sensitive signals at bottom layer
- 3rd layer for GND. The ground layer acts as a shielding to cover the signal traces at bottom layer.

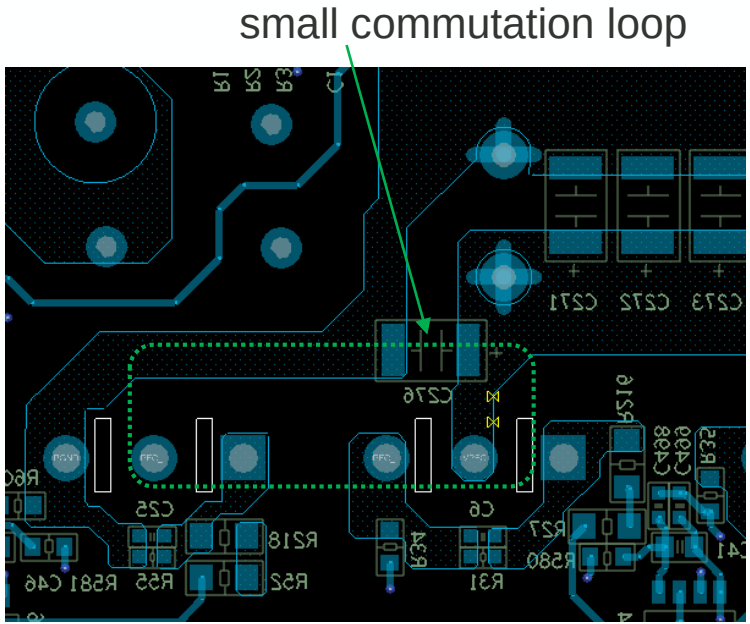
High di/dt Commutation loop

Common Mistakes:
Large commutation loop.



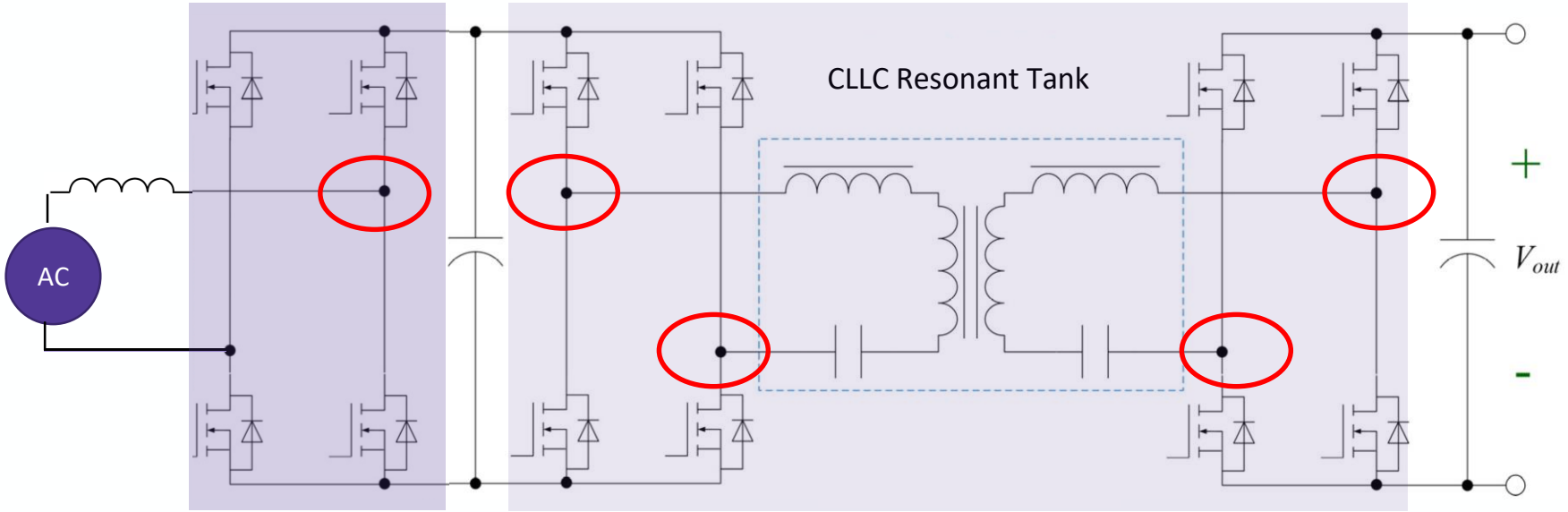
•Place ceramic or film caps as close as possible to minimize the high di/dt loop.
•Proper PCB layout of the power components to minimize the high di/dt loop.

Commutation Loop High di/dt



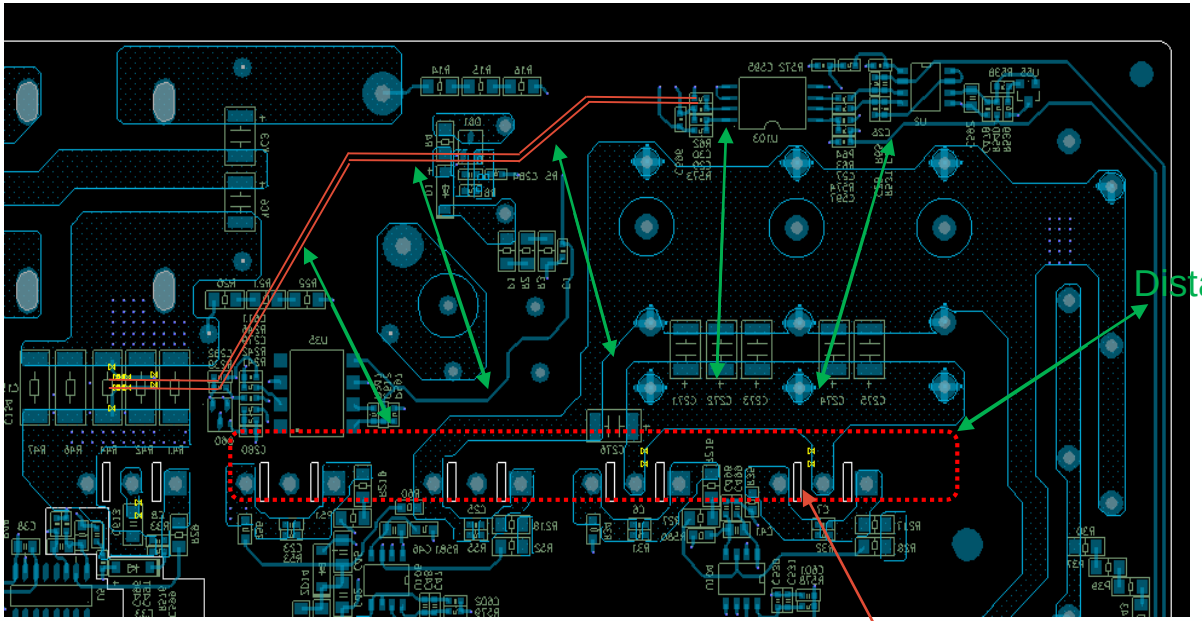
- Place ceramic or film caps as close as possible to minimize the high frequency di/dt loop.
- Proper PCB layout of the power components to minimize the high frequency di/dt loop.

High dv/dt trace/node

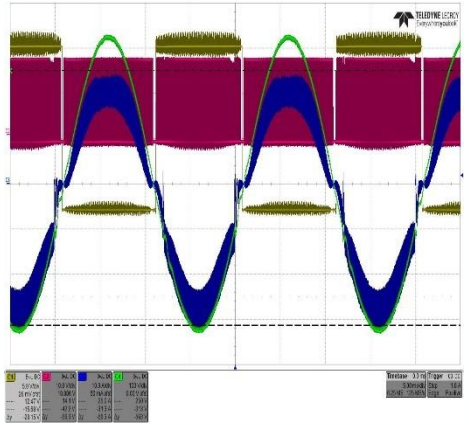


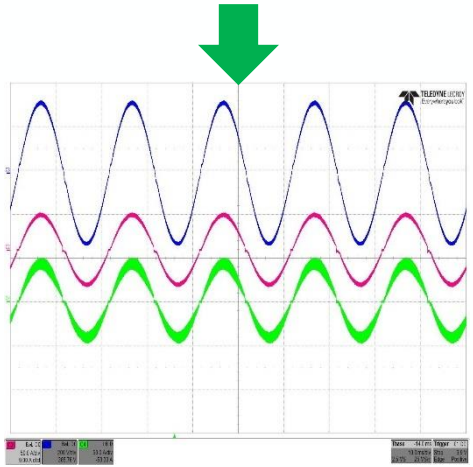
- Small pad size of Drain nodes to reduce the coupling and parasitic capacitance
- Keep the sensitive signals far away from the high dV/dt trace/nodes.
- Keep the sensitive signals far away from the high magnetic field such as PFC choke, DCDC power magnetics.

High dv/dt trace/node



Distance!





- Keep the sensitive signals far away from the high dV/dt trace/nodes.
- Keep the sensitive signals far away from the high magnetic field such as PFC choke, DCDC power magnetics.
- Small pad size of Drain nodes to reduce the coupling and parasitic capacitance

Parasitic Caps of PCB

$C = \varepsilon_r S/4\pi kd$

$1/4\pi k = 8.85\times10^{-12} F/m$

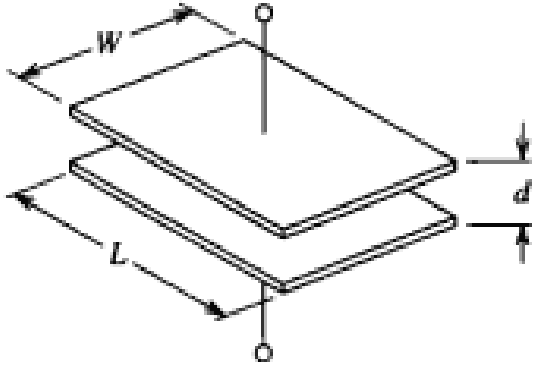
ε_r of FR4 → ~4.3

d = 0.0001m

For 1 cm ^{2} PCB trace overlap:

$C = 4.3*0.01*0.01*8.85\times10^{-12} /0.0001 = 38pF$

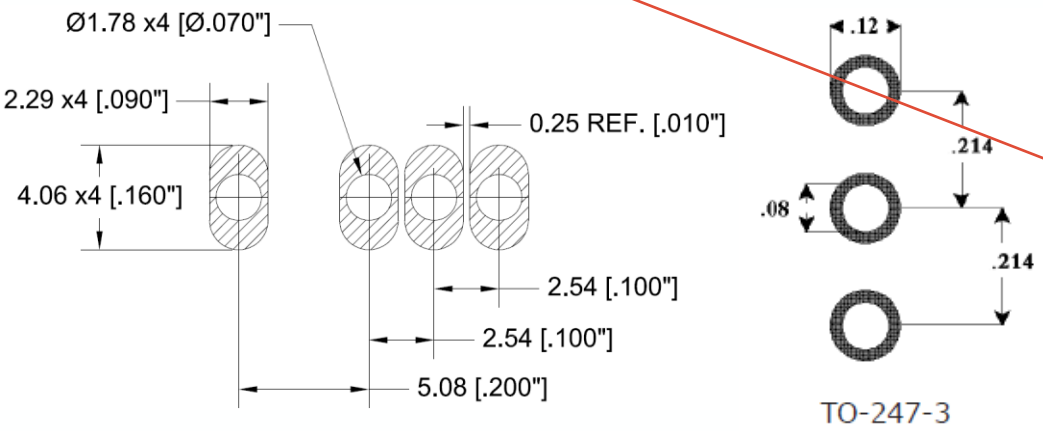
$Pc = 0.5*C*f*V^2 =$ 0.304W for 400Vbus @100kHz

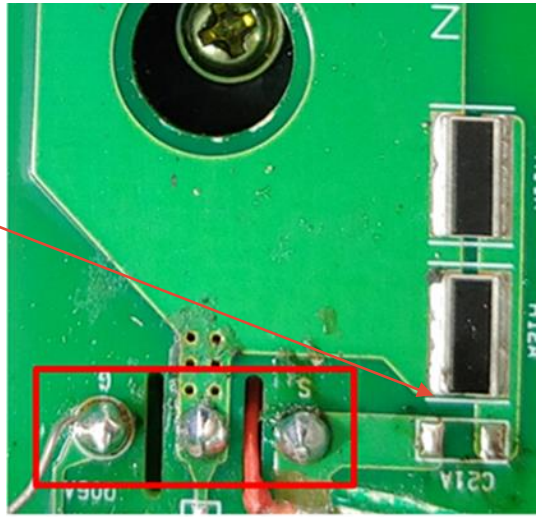


- Short and small traces to reduce the coupling and parasitic capacitance

Insufficient Creepage

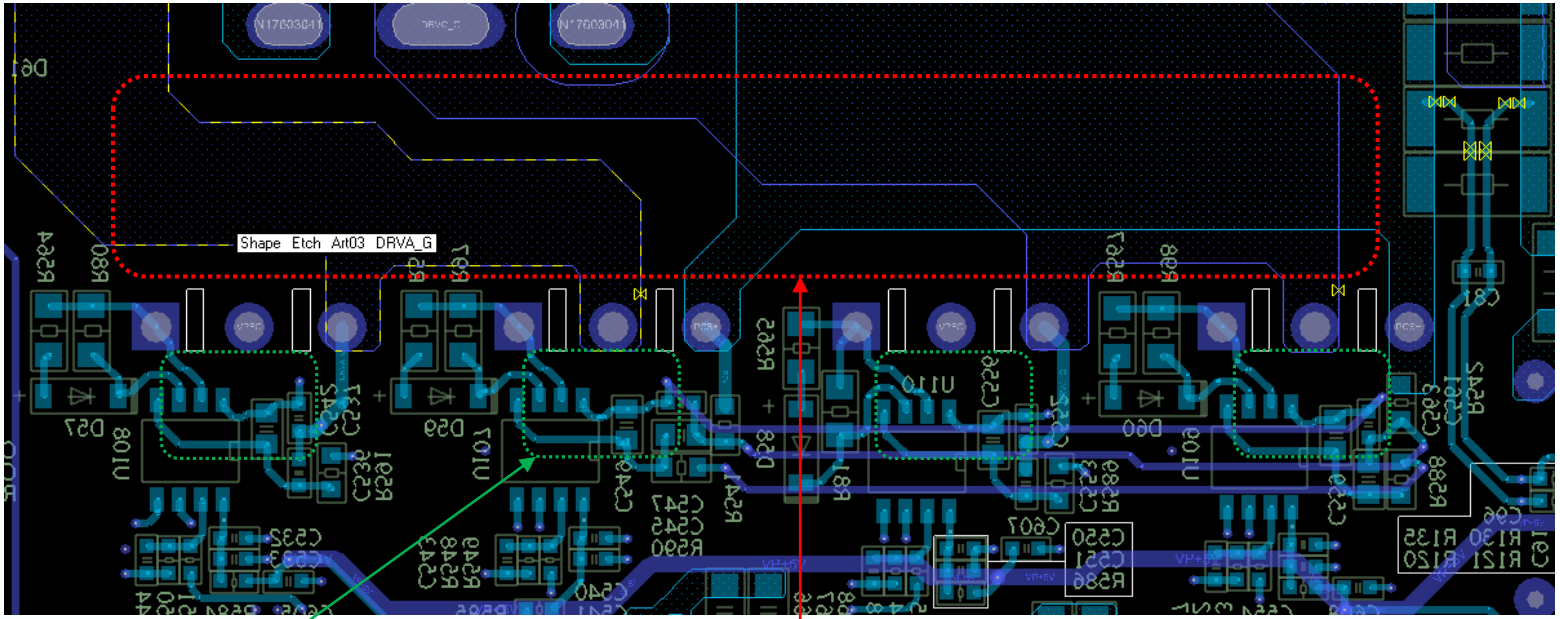
1. 8mm creepage at the body of TO-247-4 package. But the creepage between the PCB pads is only 2.3mm.2.8mm creepage for TO-247. But the creepage between the pads is only 2.38mm.
   →Need to add slots to get the required creepage
2. Snubber circuit should also follow the same rules.





No Overlap between Gate and Drain

- Avoid overlap between Drain and Gate and Gate drive circuit.

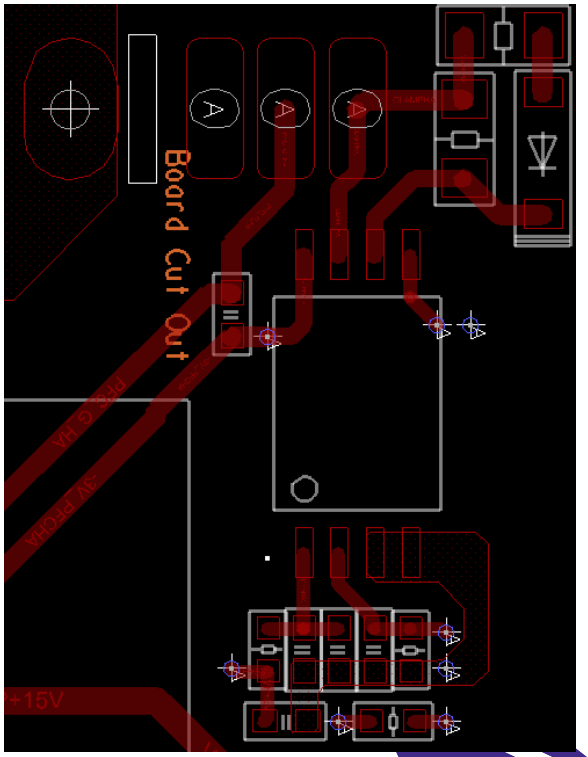


Long Distance between Gate Drive and MOSFET

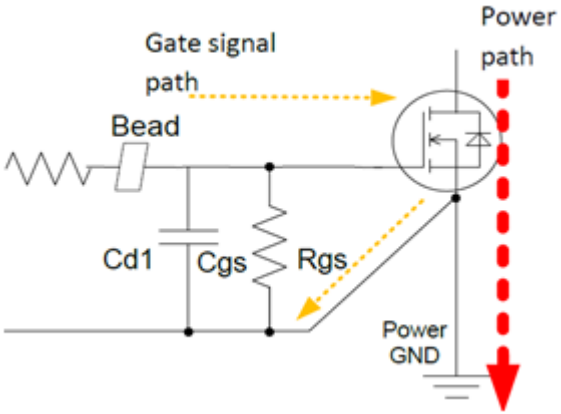
Common Mistakes: long distance between gate and MOSFET.

Tips:
Locate gate driver as close as possible to the MOSFET.
See the example.

1. Minimize the gate drive loop inductance
2. Minimize the miller clamp loop inductance
3. Place the external C or RC from **Gate to Kelven Source** as close as possible to the MOSFET



Keep the power loop separate from the gate loop

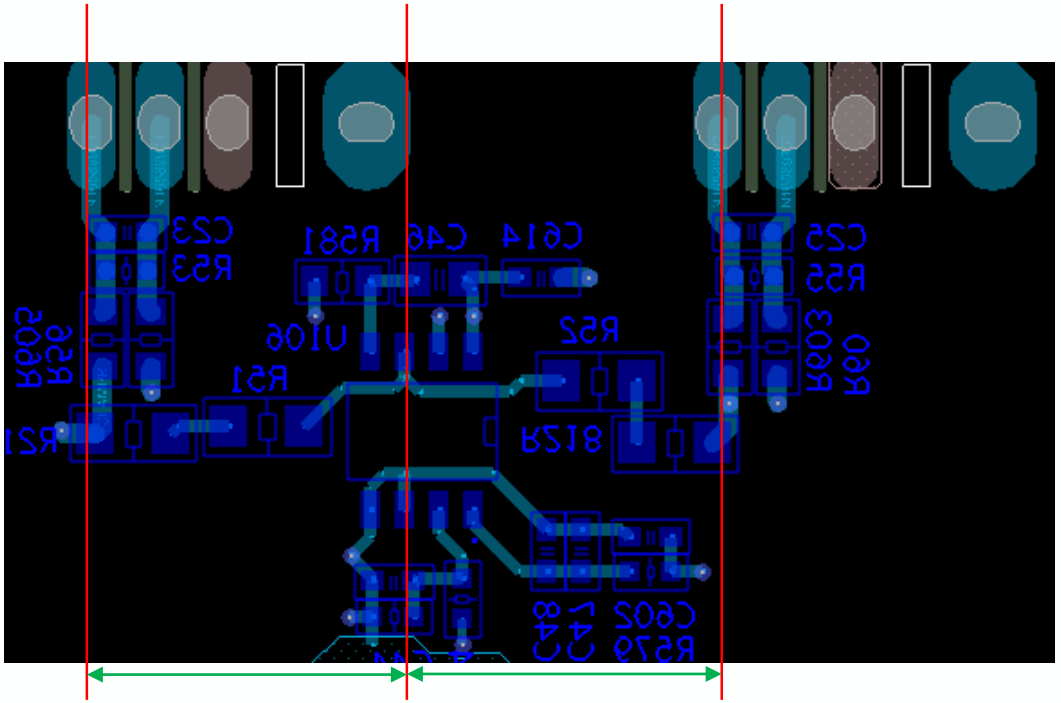


Locate gate driver as close as possible to the MOSFET

1. Use devices with Kelvin source
2. Keep the power loop separate from the gate loop for devices without Kelvin source

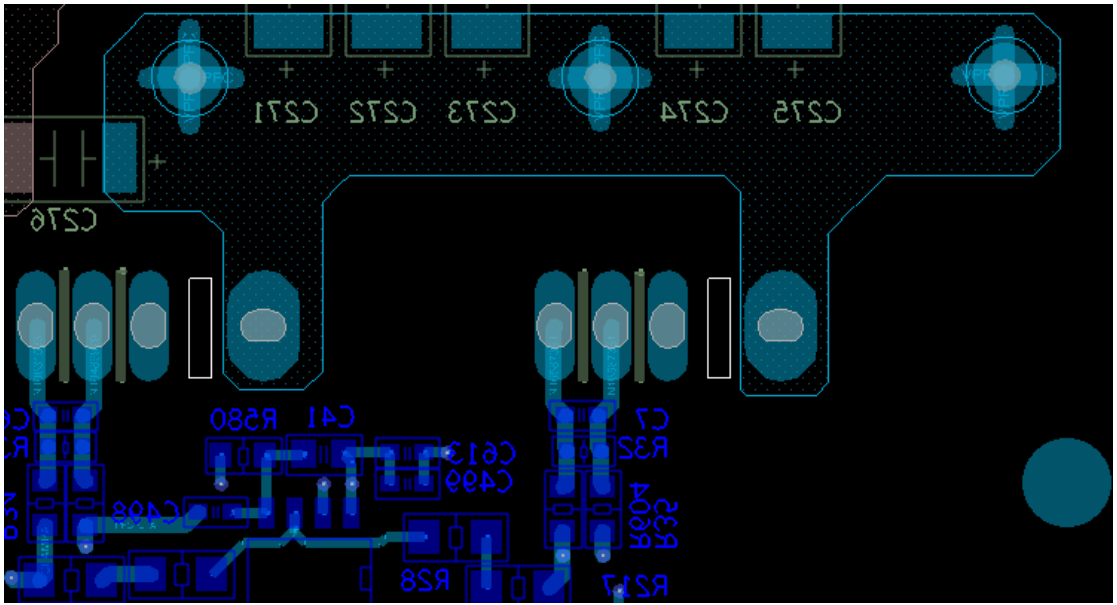
Layout example of paralleling two K-package MOSFETs

- Gate and return paths from gate driver to each MOSFET are symmetrical. Place the gate drive IC at center of two Gate pins. Not the middle of two MOSFETs.
- The length of the gate and Kelvin source runs shown are equal in length which is ideal for good current sharing.
- Have gate resistors in both Gate and Source



Layout example of paralleling two K-package MOSFETs (continued) Optimal drain and source (power) layout

- The power current path through each MOSFET should be similar in total length.
- Minimize and have balanced stray inductance at drain and gate.
- 10~20nH balancing Inductances inductance also can be considered if it is feasible.

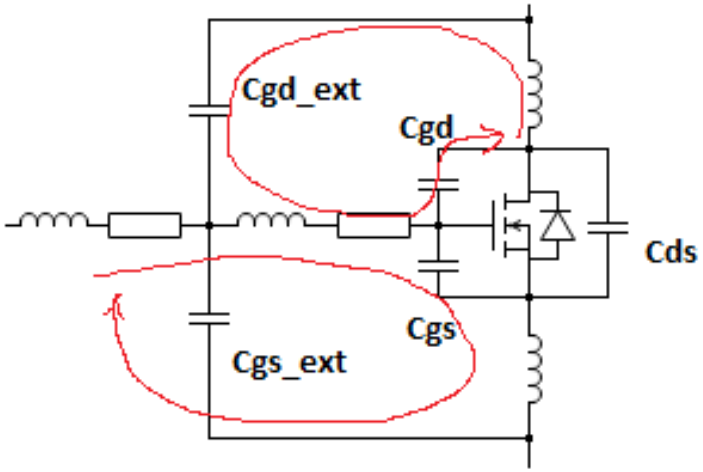


How to Reduce Gate Oscillation

Gate Oscillation

Causes:

- Fast switching of SiC MOSFET
- Parasitic capacitance and inductance, especially Common Source Inductance

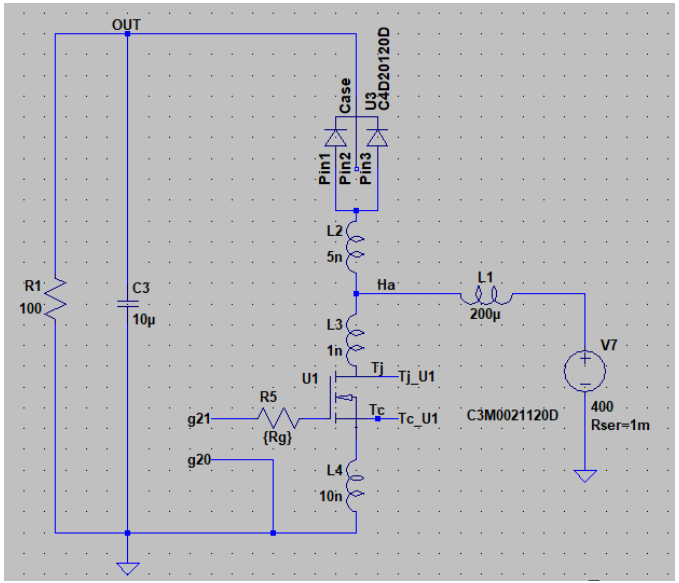


Consequences:

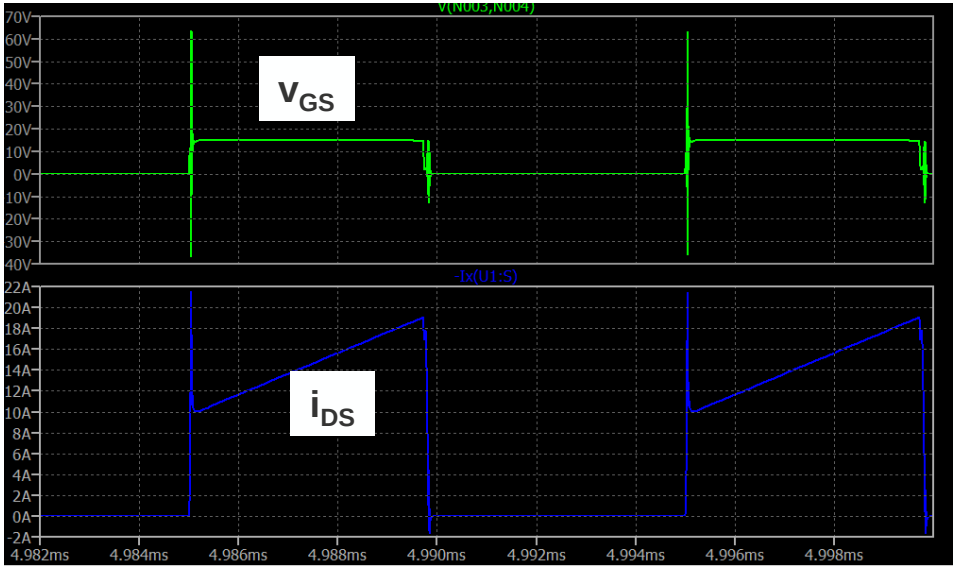
- Higher switching loss
- Gate oxide voltage breakdown
- EMI

With 0V turn-off, it is even more prone to gate oscillation.

Gate Oscillation Examples: C3M0021120D in Boost



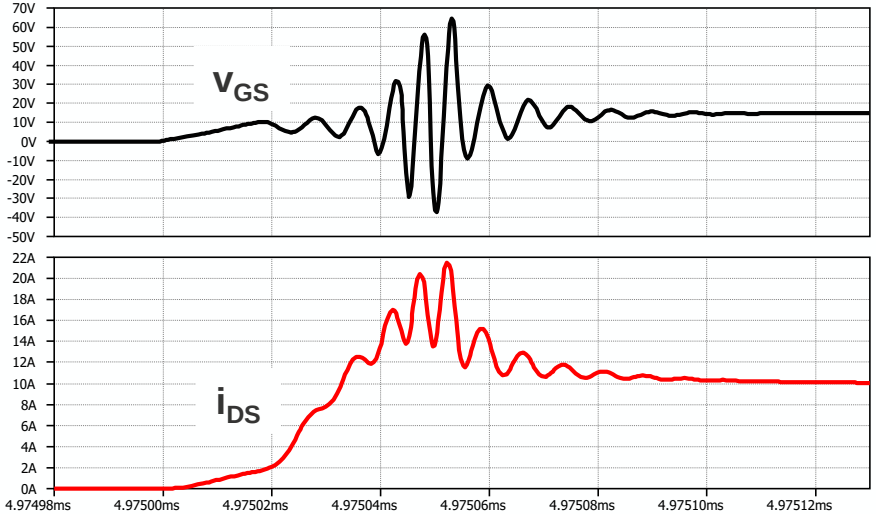
Boost
R_G = 1.5 Ω, f_s = 100 kHz,
L_S = 10 nH



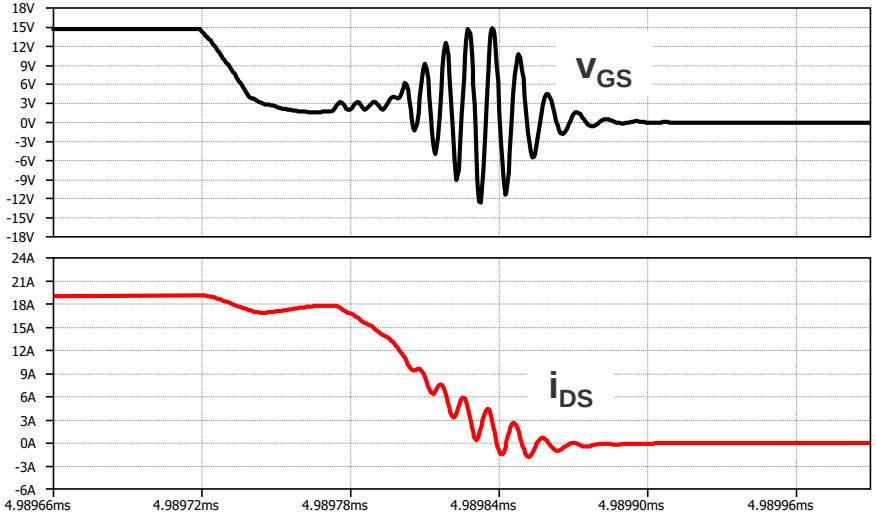
- Severe ringing of gate drive
- Oscillation frequency = 201 MHz
- Power loss of lower switch = 56.53 W

Gate Oscillation in C3M0021120D based Boost

Turn-on



Turn-off



Boost

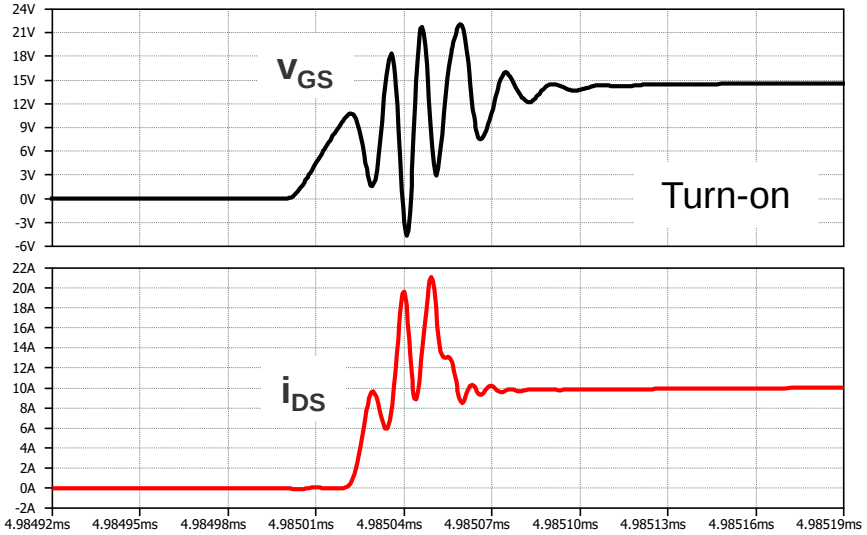
R_G = 1.5 Ω, f_s = 100 kHz,

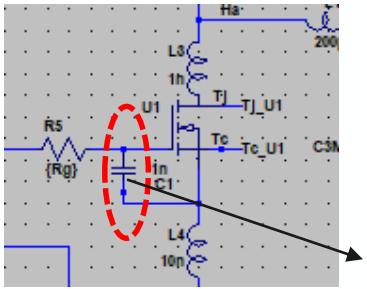
L_S = 10 nH

- Severe ringing of gate drive (peak voltage = 63V)

  Oscillation frequency = 201 MHz
- Power loss of main switch = 56.53 W

Add Capacitor at Gate and Source





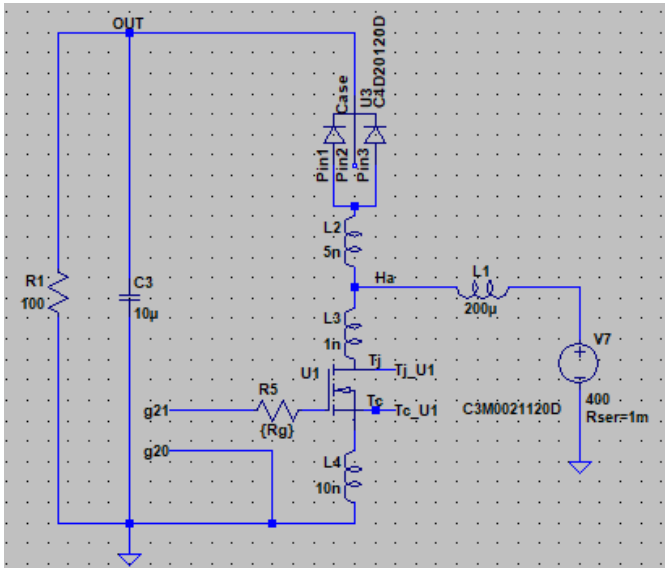
Boost
R_G = 1.5 Ω, f_s = 100 kHz,
L_S = 10 nH, C_{GS} = 1 nF

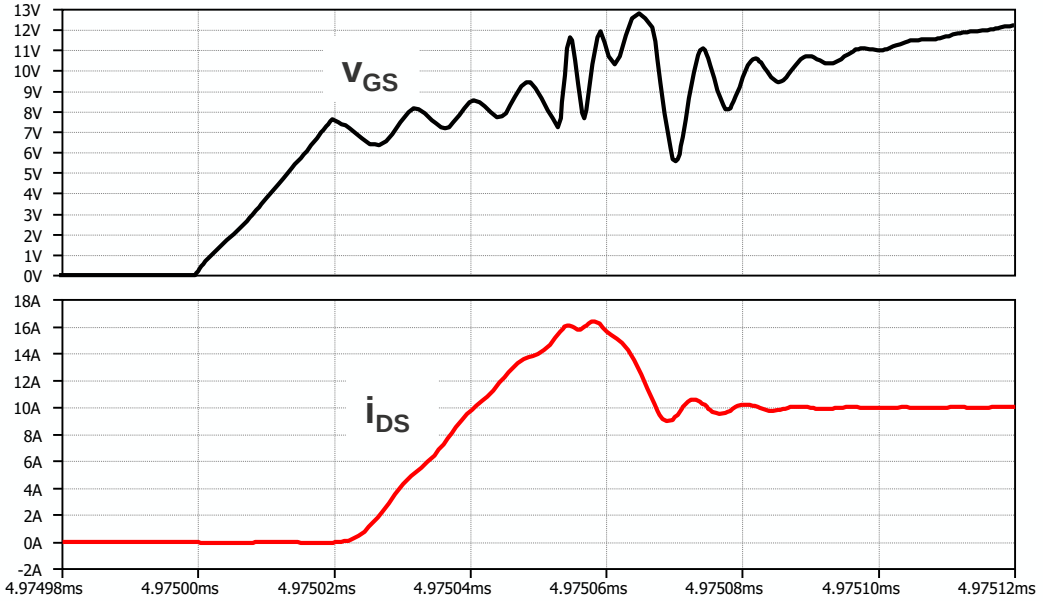
- With C_{GS} = 1nF, much less ringing of gate drive (peak voltage drop to 22V from 63V at turn-on moment)
- Oscillation frequency = 97 MHz
- Power loss of main switch = 56.55 W

Increase External R_G to Suppress Gate Oscillation

Boost

R_G = 5 Ω, f_s = 100 kHz, L_S = 10 nH



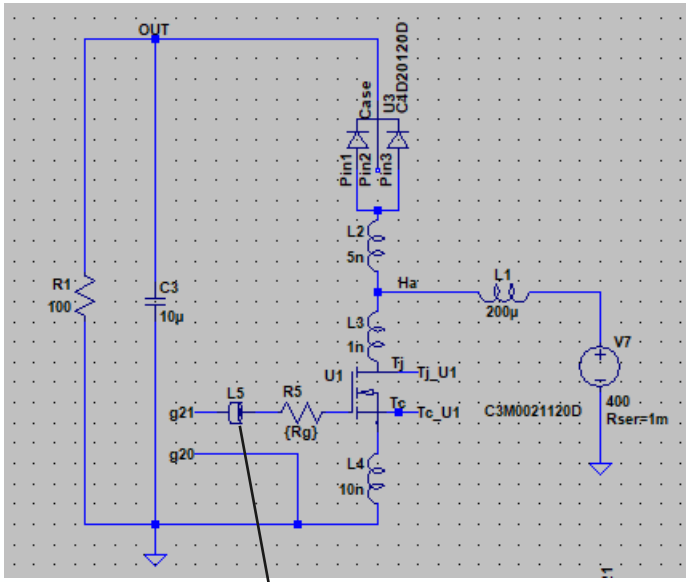


- No severe ringing of gate drive (peak voltage = 14.84V at turn-on moment)
- Power loss of main switch = 70.02 W

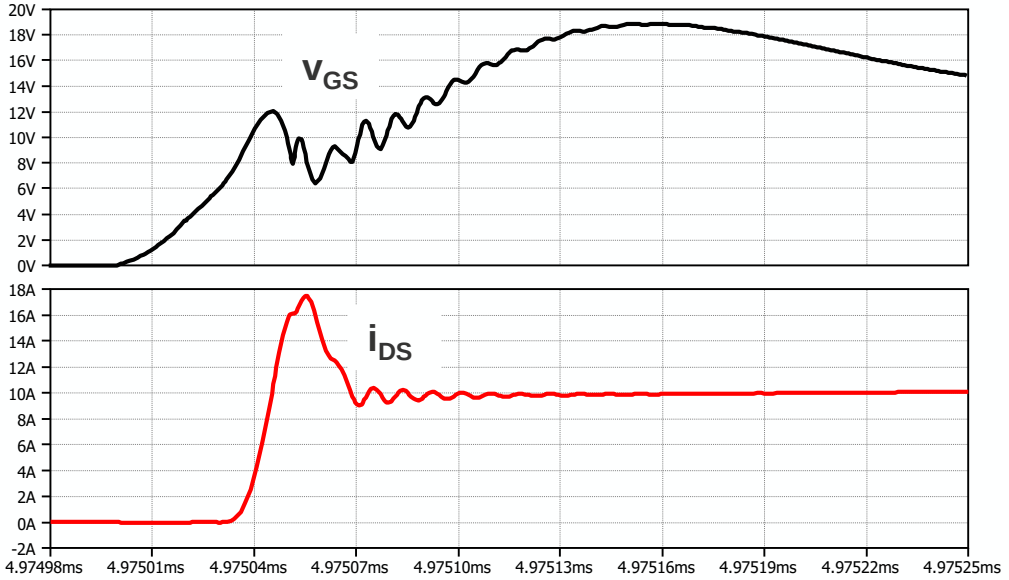
Ferrite Bead to Suppress Gate Oscillation

Boost

R_G = 1.5 Ω, f_s = 100 kHz, L_S = 10 nH



Ferrite bead (782853680 from Wurth)

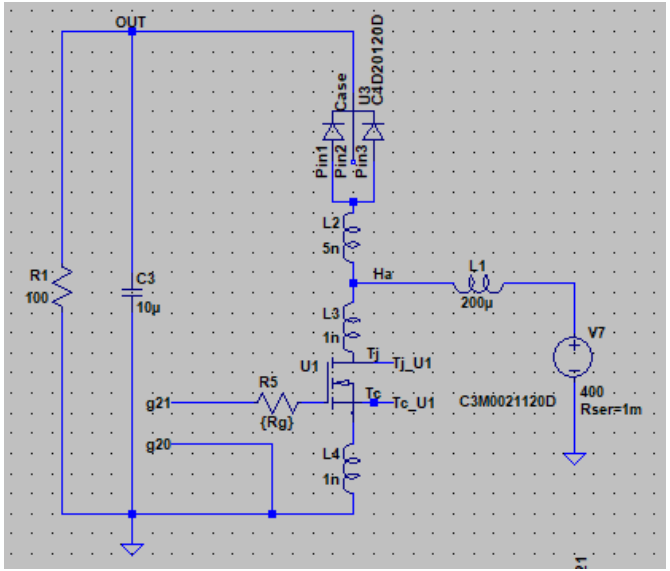


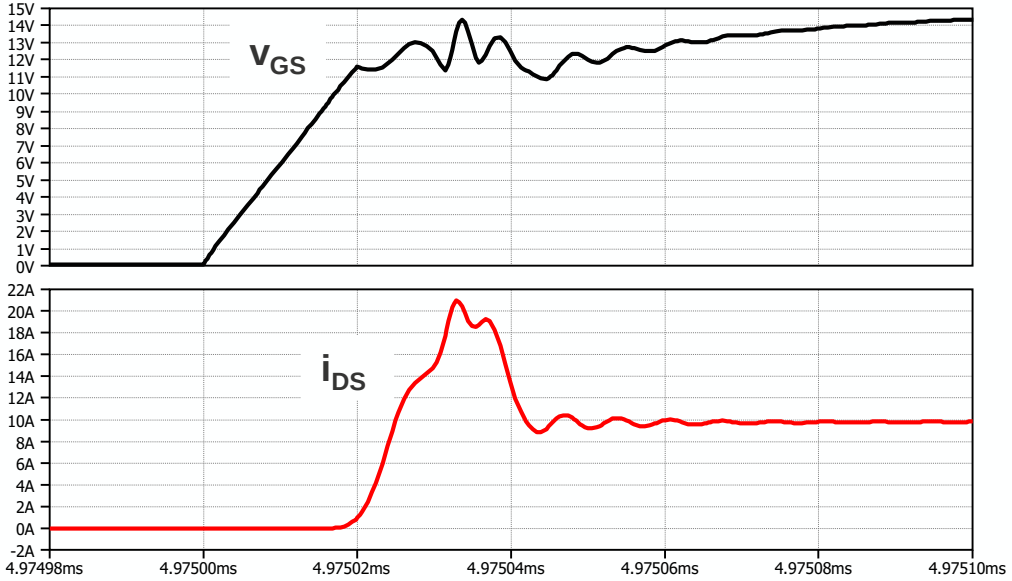
- No severe ringing of gate drive (peak voltage = 18.85V at turn-on moment)
- Power loss of main switch = 56.70 W
- Effective way of suppressing oscillation

Reduce Common Source Inductance

Boost

R_G = 1.5 Ω, f_s = 100 kHz, L_S = 1 nH



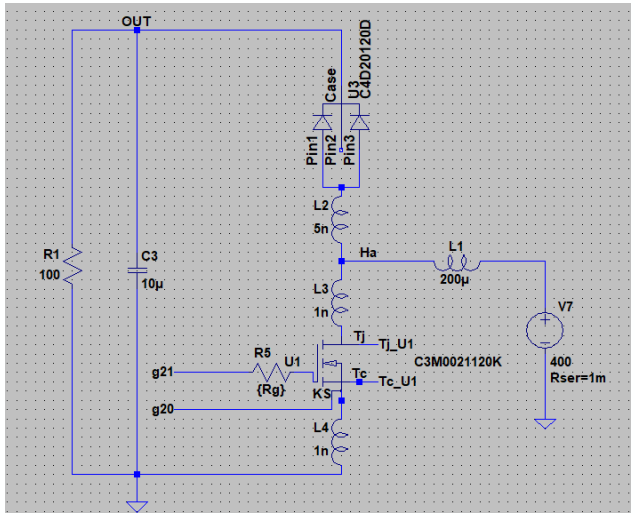


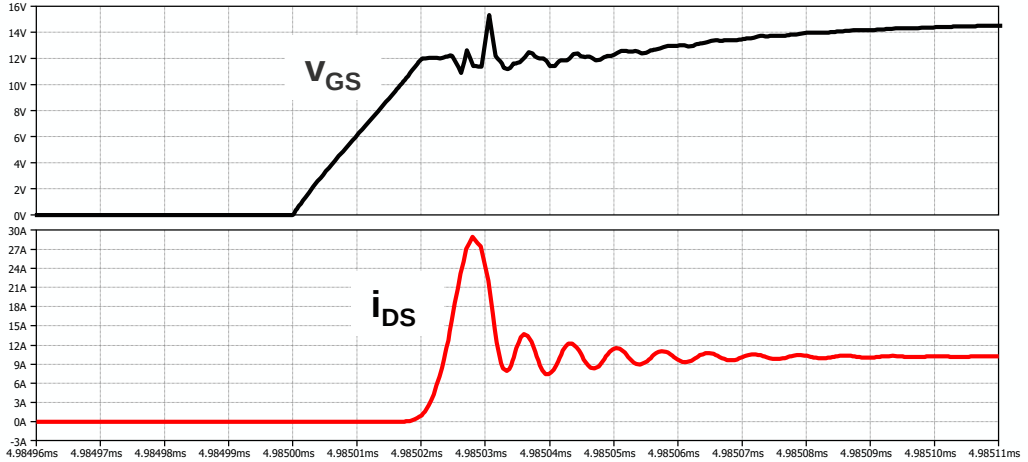
- No severe ringing of gate drive (peak voltage = 14.88V at turn-on moment)
- Power loss of main switch = 32.52 W

Use Kevin Source Package Device with reduced Common Source Inductance

Boost

R_G = 1.5 Ω, f_s = 100 kHz, L_S = 1 nH





- Less severe ringing of gate drive (peak voltage = 15V at turn-on moment)
- Power loss of main switch = 23.87 W

Summary: Gate Oscillation Mitigation

- Use of Kevin source package
- Reduce common source inductance
- Add C or RC between Gate and KS
- Proper R_G
- Use of ferrite bead