Cost-Effective Method to Discharge DC Link Capacitors with SiC Power Modules

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Abstract

The high bus voltages commonly used in electric vehicles (EVs) present a safety hazard to vehicle operators and technicians. As the number of EVs on the road increases, it is essential to mitigate these risks by implementing safety features to prevent contact with high-voltage conductors within the vehicle. The primary source of shock risk within the vehicle is from the DC link capacitors that source energy from the EV batteries to the inverter. These capacitors must be discharged when the vehicle is not in operation, such as when the vehicle is turned off or in the event of a crash. This paper presents an active discharge technique that dissipates the DC link energy through the switching semiconductors already present in the system, thus not requiring additional components or control circuitry. The proposed method works by commanding the inverter to alternate between zero sequence states at a high switching frequency. The output capacitance (C_{OSS}) of the power devices are charged and discharged each switching period to dissipate the energy stored in the DC link capacitors across the power module. This method is advantageous because the discharge rate is easily controlled and limits thermal heating within the MOSFETs. This paper demonstrates the operation of this method using a SiC power module and presents an analytical model for predicting the discharge time of the DC link capacitor. The analytical model is shown to accurately predict the discharge time for a given system. The power dissipated in the modules during the discharge event is also evaluated and shown to be well within the allowable operating conditions of the power module.

1 Introduction

As EV manufacturers strive to maximize range and efficiency in electric vehicles, 800 V vehicle powertrain designs are becoming increasingly common [1], [2]. The higher voltages and large DC link capacitances required for the inverter subsystem can present life-threatening shock, as stated by IEC 60479-2 [3]. Therefore, methods to quickly and reliably discharge the DC link capacitors when the vehicle is not in operation are necessary. Currently, two primary methods are used to discharge the DC link capacitors. The first is a simple method that uses a switch to connect a resistive element across the DC bus to dissipate the energy, as shown in Fig. 1. While this method is effective, it is expensive and adds at least two failure points to the inverter system.

A second method commonly proposed in literature uses advanced control schemes to discharge the DC link capacitors energy in the motor windings [4], [5], [6], [7]. However, these methods require that the load be connected, functional, and energized. This paper purposes a novel method for discharging the DC link capacitors that does not require additional components or a functional load, and only requires use of the power switching devices. The discharge is achieved by alternating between zero sequence states and using the device output capacitance to discharge the DC link capacitors.

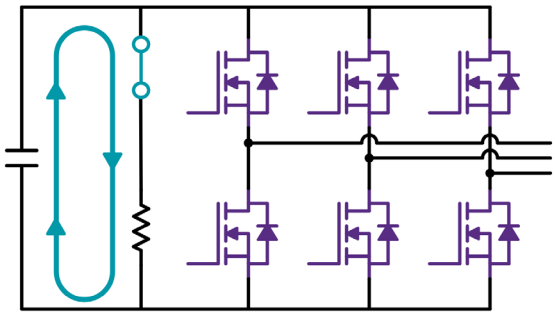

Fig. 1 Simple Resistive Discharge Method

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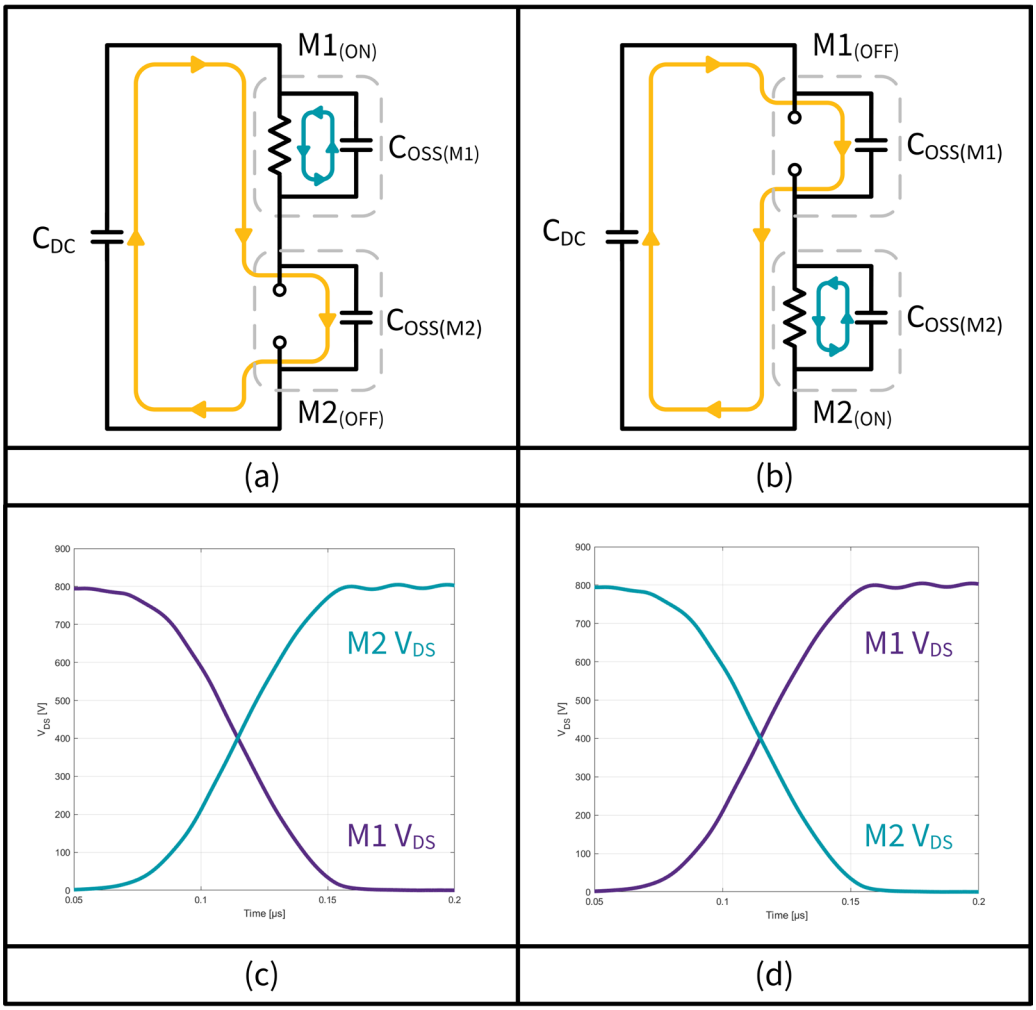

Fig. 2 Half-bridge power module model architecture [3]

2 Theory of Operation

The proposed discharge method involves commanding each phase in the inverter to alternate between zero sequence states each period. At no point during the sequence can DC current flow through the switches; at least one switch position is blocking at all times. For the first half of the period, all high-side switches are on and all low-side switches are off. For the second half of the period, all low-side switches are on and all high-side switches are off. This process sequentially charges and discharges the output capacitance of the power MOSFETs. During the first half of the period shown in Fig. 2 (a), the high-side switch is turned on by the gate driver. In this state, $C_{OSS(M2)}$ charges up to the bus voltage. The energy stored in $C_{OSS(M1)}$ along with the additional current required to charge $C_{OSS(M2)}$ is dissipated as heat across device M1. During the second half of the period shown in Fig. 2 (b), $C_{OSS(M1)}$ is charging, and the energy stored in $C_{OSS(M2)}$ along with the additional current required to charge $C_{OSS(M1)}$ is dissipated as heat across device M2. This leads to two instances of the MOSFET's stored energy due to the output capacitance, E_{OSS}, being removed from the DC link capacitor for each half-period. Therefore, four times E_{OSS} is removed from the DC link capacitor for each switching period. Note that the currents shown in Fig. 2 (a) and Fig. 2 (b) are only flowing during the dv/dt events shown in Fig. 2 (c) and Fig. 2 (d), respectively. V_{DC} is the voltage across the module defined in (1).

$$V_{DC} = V_{M1} + V_{M2} \quad (1)$$

2.1 Energy Loss Per Switching Period

For each switching period the voltage transitions shown in Fig. 2 (c) and Fig. 2 (d) occur corresponding to the switch states in Fig. 2 (a) and Fig. 2 (b). Once the voltage has transitioned, there is no current flowing from C_{DC}. Fig. 2 (a) shows the time period where M1 is on and M2 is off. Prior to the switching event, $C_{OSS(M1)}$ is charged and has potential energy stored equal to (2). Switch M1 is turned on and the output capacitance of M2 charges to V_{DC}. Once charged it will have taken energy from the bus C_{DC} and stored it as potential energy in accordance with (3).

$$E_{COSS(M1)} = \frac{1}{2} \cdot Q_{OSS(M1)} \cdot V_{M1,t0} \quad (2)$$

$$E_{COSS(M2)} = \frac{1}{2} \cdot Q_{OSS(M2)} \cdot V_{M2} \quad (3)$$

The change in voltage across the module (V_{DC}), is very small due to the capacitance of C_{DC} being much larger than C_{OSS} (4).

$$C_{DC} \ggg C_{OSS} \quad (4)$$

From (4), we make the simplifying assumption that the change in voltage across C_{DC} (V_{DC}) is zero during the charge time of $C_{OSS(M2)}$. With this simplifying assumption, the total energy loss from C_{DC} can be calculated with (5).

$$\Delta E_{DC} = Q_{OSS} \cdot V_{DC} \quad (5)$$

Knowing that half of the energy lost from C_{DC} is stored in $C_{OSS(M2)}$ as potential energy (3), we know the other half of the energy lost from C_{DC} is dissipated as heat across M1. However, the total amount of energy dissipated across M1 must include the energy stored in $C_{OSS(M1)}$. The total amount of energy dissipated as heat in M1 is given in (7).

$$E_{M1(Heat)} = 2 \cdot \frac{1}{2} \cdot Q_{OSS} \cdot V_{DC} \quad (6)$$

$$E_{M1(Heat)} = Q_{OSS} \cdot V_{DC} \quad (7)$$

During each switching event, the energy removed from the DC link capacitor is given in (5) and is dissipated across the activated switch position. For Fig. 2 (a), heat is dissipated across M1, and for Fig. 2 (b), heat is dissipated across M2.

V_{DC} (V)	C_{DC} (µF)	F_{SW} (kHz)	$F_{SW,Step}$ (kHz)
1000	181	10-100	10
800	181	10-100	10
600	181	10-100	10

Table 1 Test Matrix

2.2 Temperature Rise per Discharge

The total power dissipated in the switch for each discharge cycle is given by (8). From that we can estimate the average die temperature increase from the R_{TH} of the system with (9).

$$P_{Loss} = \frac{\frac{1}{2} \cdot C_{DC} \cdot V_{DC}^2}{Discharge\ Time\ [s]} \quad (8)$$

$$\Delta T_j = R_{TH} \cdot P_{Loss} \quad (9)$$

For a 2 mF DC discharged in one second across three half bridge modules with an R_{TH} of 0.15 (K/W) per position the expected temperature rise is 16 °C.

3 Results

Testing was performed using a modified version of the Wolfspeed KIT-CRD-CIL12N-XM3 evaluation board with a single DC link capacitor (shown in Fig. 3) and an EAB450M12XM3 (shown in Fig. 4). Key parameters of the test setup were measured including the capacitance of the DC link capacitor and output capacitance of the EAB450M12XM3.

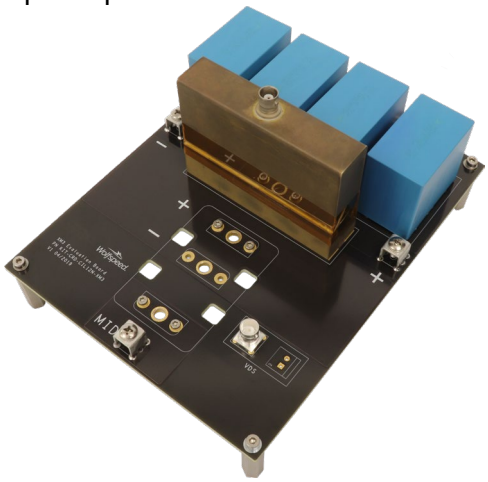

Fig. 3 KIT-CRD-CIL12N-XM Clamped Inductive Load (CIL) evaluation kit for XM3 power modules

Fig. 4 EAB450M12XM3 Half Bridge Silicon Carbide (SiC) Power Module

The test matrix consisted of three DC link voltages 1000 V, 800 V, and 600 V. For each voltage, the discharge time is defined from the starting voltage to 50 V. Each test was performed for switching frequencies from 10 kHz to 100 kHz with a 10 kHz increment.

3.1 Test Setup

The XM3 power module was mounted to the KIT-CRD-CIL12N-XM CIL board. A CGD12HBXMP gate driver was attached to the module to control the gates. The CIL board was connected to the high voltage dc supply through the relay and control board to charge the DC link capacitors. Fig. 5 shows a simplified block diagram of the test setup.

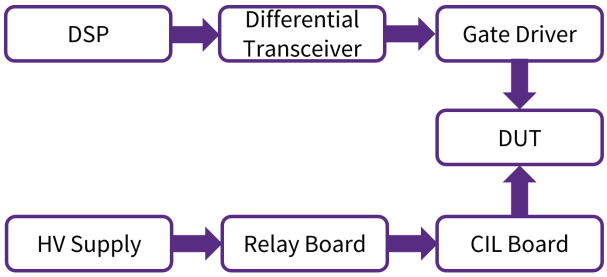

Fig. 5 Test Setup Signal Chain

Fig. 6 Shows the actual test setup with annotations describing each component.

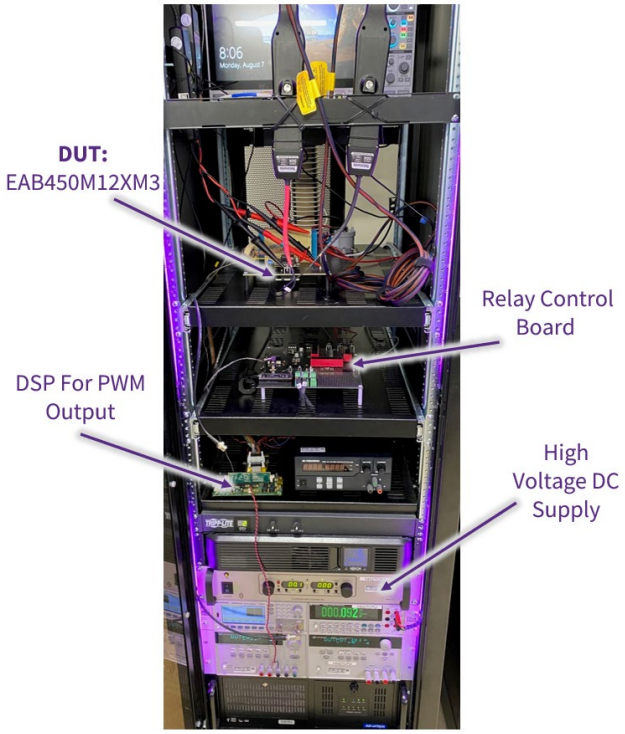

Fig. 6 Experimental Test setup

3.2 Test Sequence

The DC link capacitor was charged by a high voltage power supply through the relay control board. Once charged, the relays were opened, disconnecting the CIL board from any galvanic ground connections. The DSP initiates the test by sending the complementary PWM signals to the gate to discharge the bus. The entire discharge event is captured on the oscilloscope and the discharge time is measured Fig. 7.

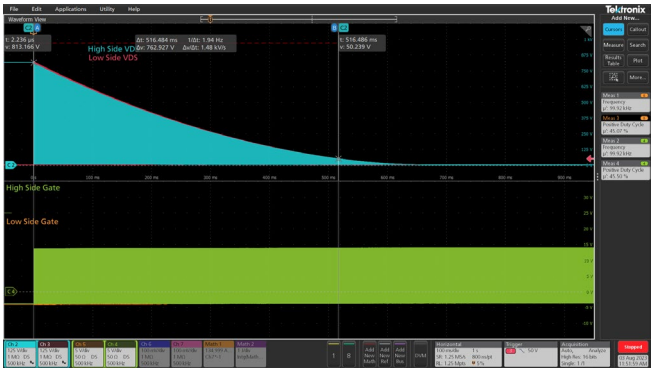

Fig. 7 Example of Discharge Event

The process was repeated for all conditions in the test matrix Table 1.

3.3 Experimental Results

The discharge times for each of the test conditions is plotted in Fig. 8. The discharge time reduces proportionally to the increased switching frequency as expected from the theoretical understanding of the discharge event.

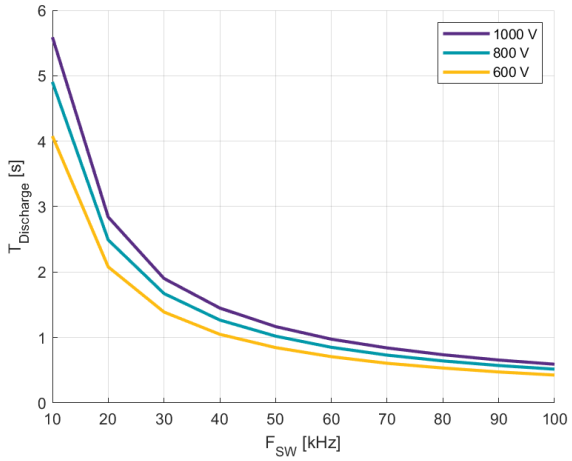

Fig. 8 DC Link Discharge Time vs. F_{SW}

4 Analytical Model

An analytical model was created to estimate the discharge time for different configurations of DC link capacitance and number of modules. The model was verified against the experimental test results and was proven to accurately predict the discharge time.

4.1 Model Operation

For each switching period, E_{OSS} of the module is calculated based on the C-V characteristics of the power module. The C-V characteristics of the EAB450M12XM3 power module is shown in Fig. 9. The initial energy stored in the DC link capacitor is calculated based on the current bus voltage (10). Four times E_{OSS} (2) is subtracted from the energy stored in the DC link capacitor.

$$\mathrm{E}_{DC,Initial} = \frac{1}{2} \cdot C_{DC} \cdot V_{DC}^2 \qquad (10)$$

The new energy stored in the DC link capacitor is calculated with (11) and the new voltage of the DC link capacitor is calculated with (12).

$$E_{DC,New} = E_{DC,Initial} - 4 \cdot E_{OSS} \qquad (11)$$

The discharge time is increased by one period and the process repeats until the new DC link voltage is less than or equal to the target stop voltage (50 V).

$$\mathrm{V}_{DC,New} = \sqrt{\frac{E_{DC,New}}{\frac{1}{2} \cdot C_{DC}}} \qquad (12)$$

The CIL board used to perform the experimental tests contained bleed resistors to discharge the DC link capacitor in the event of a test failure.

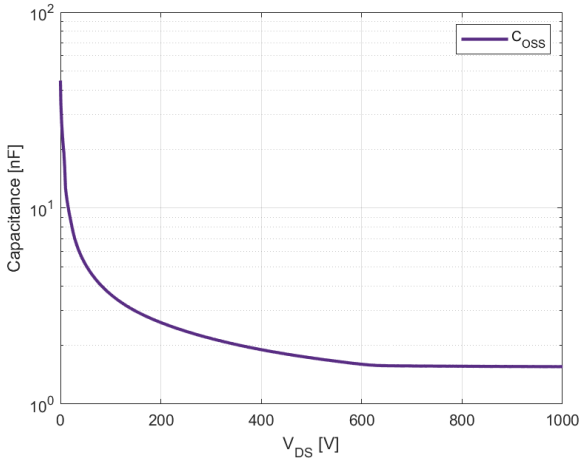

Fig. 9 C_{OSS} vs. V_{DS} for an EAB450M12XM3 power module

4.2 Model Validation

Average Percent Error	0.352
Standard Deviation of Percent Error	0.610
Variance of Percent Error	0.372

Table 2 Summary of Model Accuracy

To validate the model, the experimental test results for a starting DC link voltage of 800 V were compared to the simulated results produced by the analytical model.

The results for each of the ten test conditions are given in Table 1 and a summary of the results are given in Table 2 and Table 3.

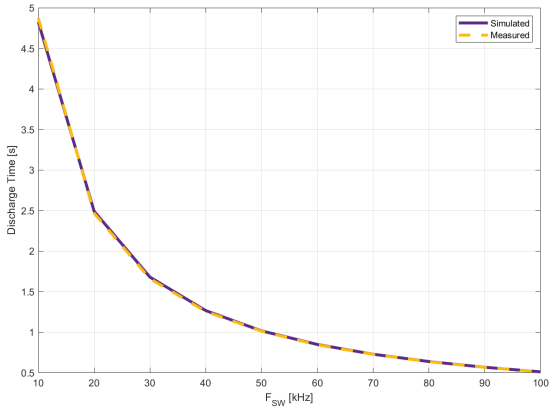

Fig. 10 Simulated Discharge vs. Measured Discharge time

The analytical model results in an average of less than one percent error across the test conditions. That error is likely to be due to extra capacitance in the CIL board not captured by the analytical expressions.

5 Conclusion

The active discharge method proposed in this paper operates the power modules in a mode that matches the intended use of the devices by switching completely from the negative V_{GS} to positive V_{GS}. The DC link capacitors can be fully discharged in under one second by increasing the switching frequency. The temperature rise of the power module is well within the operating limits of the power modules.

With the increasing demand to find a solution to discharge the DC link capacitance in electric vehicles, this method is viable.

Alternating between zero sequence states at elevated switching frequencies provides a low cost, predictable method for discharging the DC link capacitance. The analytical method described in this paper can be used to predict the discharge time for a given system.

F_{SW} (kHz)	$T_{Dis,sim}$ (ms)	$T_{Dis,exp}$ (ms)	Error (%)
10	4824	4872	0.99
20	2491	2468	-0.93
30	1679	1660	-1.17
40	1267	1257	-0.83
50	1017	1012	-0.46
60	849	844	-0.56
70	729	727	-0.21
80	639	637	-0.24
90	568	567	-0.23
100	512	512	0.12

Table 3 Results Comparison

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