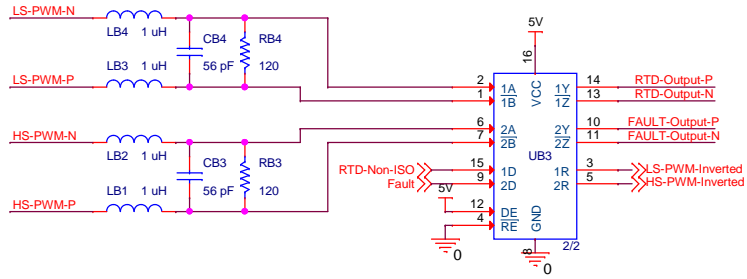
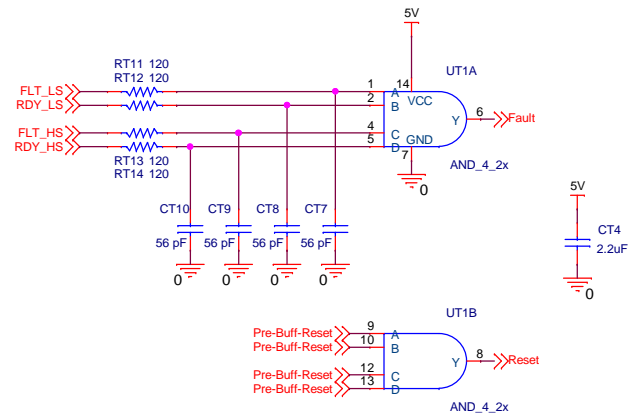


DIFFERENTIAL TRANSCIEVER

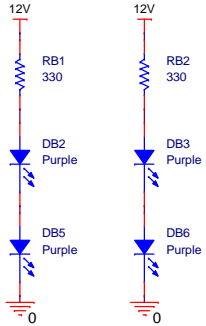


The default output of the differential transceiver is high if the inputs are left open. To ensure that the gate driver output is not driven high during this state, the positive and negative lines of the differential signal are flipped, which inverts the PWM signals.

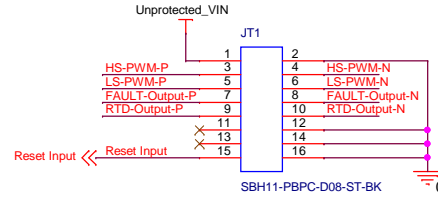
FAULT COMBINATION



UNDERGLOW

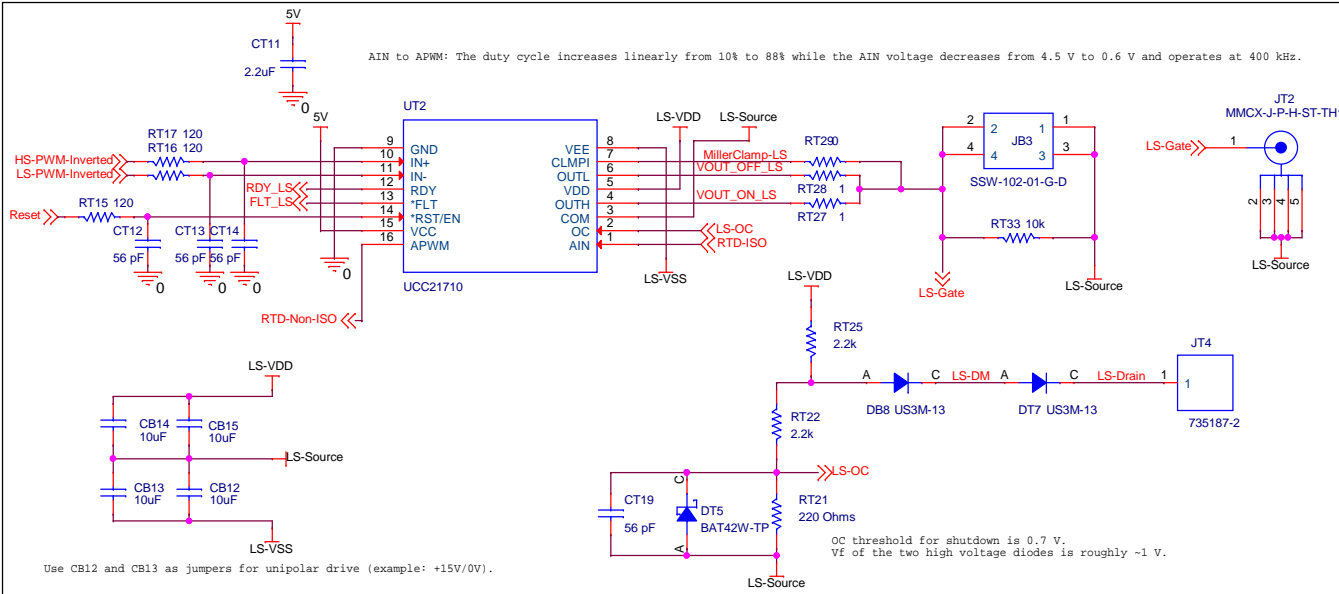


I/O



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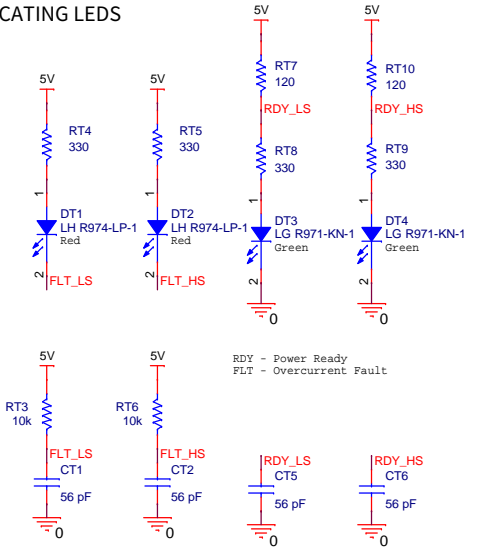
AIN to APWM: The duty cycle increases linearly from 10% to 88% while the AIN voltage decreases from 4.5 V to 0.6 V and operates at 400 kHz.



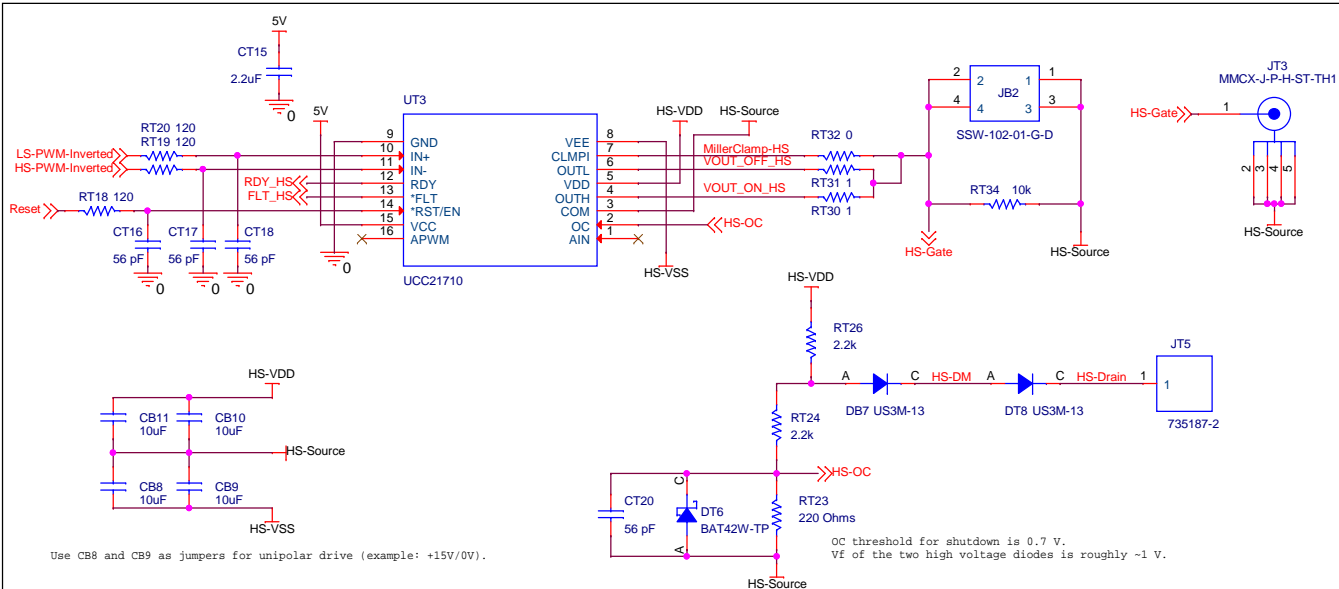
Use CB12 and CB13 as jumpers for unipolar drive (example: +15V/0V).

LOW SIDE DRIVER

FAULT INDICATING LEADS



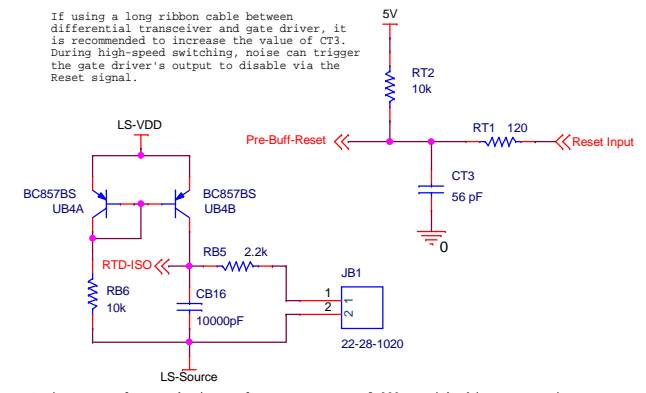
RDY - Power Ready
FLT - Overcurrent Fault



Use CB8 and CB9 as jumpers for unipolar drive (example: +15V/0V).

HIGH SIDE DRIVER

If using a long ribbon cable between differential transceiver and gate driver, it is recommended to increase the value of CT3. During high-speed switching, noise can trigger the gate driver's output to disable via the Reset signal.

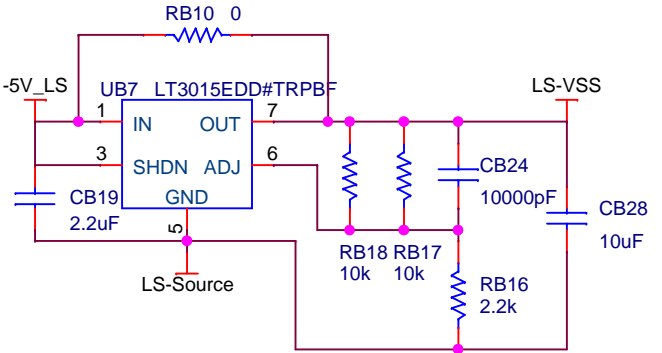
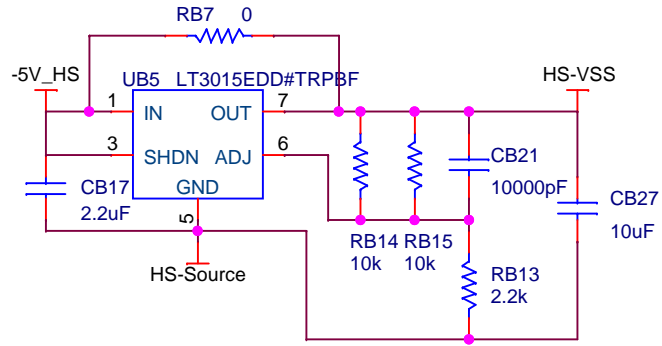


Option to supplement the internal current source of 200 μ A with this current mirror.

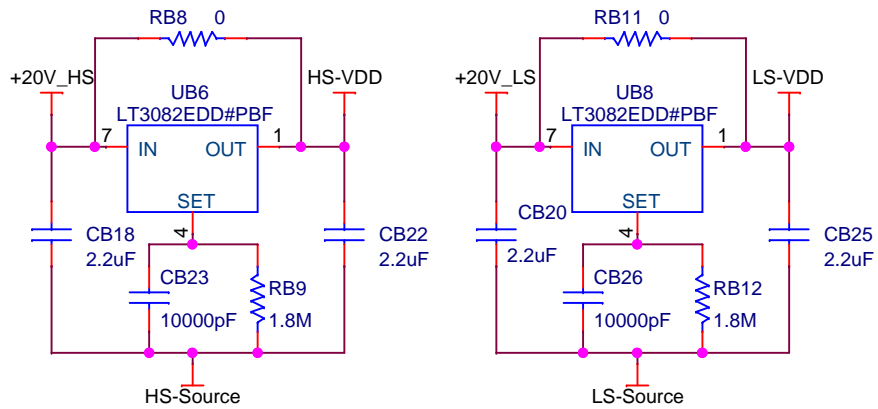
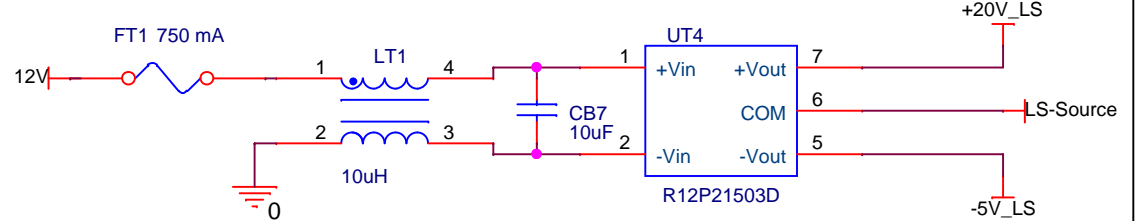
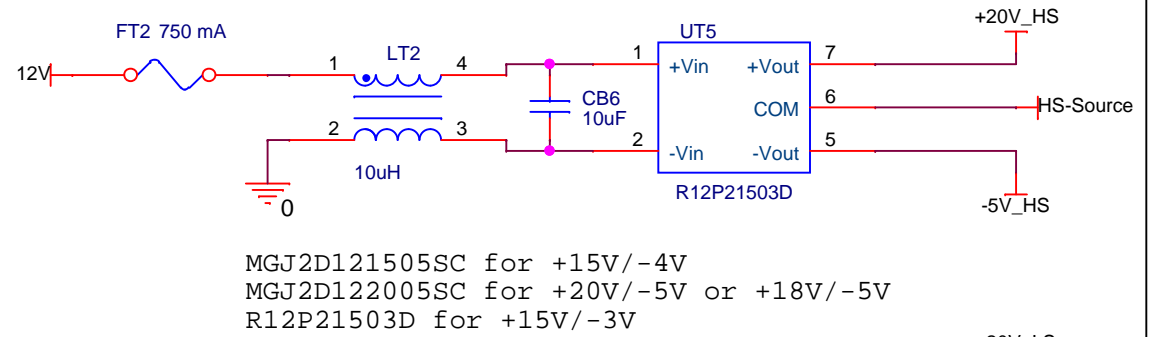


Title		Gate Drivers	
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Negative Regulators

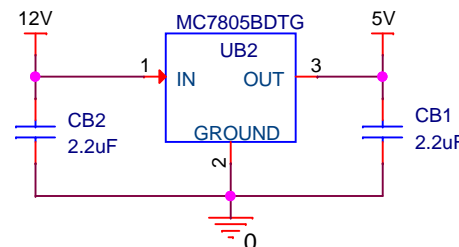


Isolated DC/DC Converters

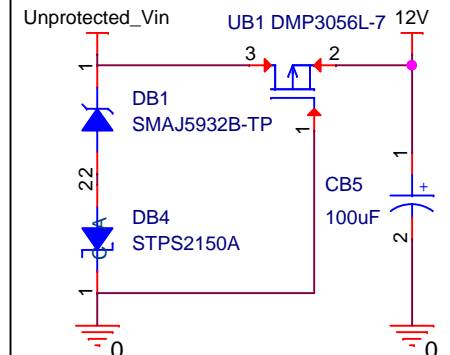


Positive Regulators

+5 V Primary Regulator



Input Protection



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