

CRD-06600FF10N 6.6 kW BI-DIRECTIONAL EV ON-BOARD CHARGER

CRD-06600FF10N
6.6kW 双向电动车载充电器

CRD-06600FF10N
6.6kW 双方向 EV オンボード 充電器



Application Note CPWR-AN24, Rev- Cree Power Applications

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- **Death**
- **Serious injury**
- **Electrocution**
- **Electrical shock**
- **Electrical burns**
- **Severe heat burns**

You must read this document in its entirety before operating this board. It is not necessary for you to touch the board while it is energized. All test and measurement probes or attachments must be attached before the board is energized. You must never leave this board unattended or handle it when energized, and you must always ensure that all bulk capacitors have completely discharged prior to handling the board. Do not change the devices to be tested until the board is disconnected from the electrical source and the bulk capacitors have fully discharged.

警告

请勿在通电情况下接触板子，在处理板子前应使大容量电容器完全释放电力。接通电源后，该评估板上可能存在非常高的电压，板子上一些组件的温度可能超过 50 摄氏度。此外，移除电源后，上述情况可能会短暂持续，直至大容量电容器完全释放电量。

操作板子时应确保遵守正确的安全规程，否则可能会出现下列危险：

- 死亡
- 严重伤害
- 触电
- 电击
- 电灼伤
- 严重的热烧伤

请在操作本板子前完整阅读本文件。通电时不必接触板子。在为板子通电前必须连接所有测试与测量探针或附件。通电时，禁止使板子处于无人看护状态，或操作板子。必须确保在操作板子前，大容量电容器释放了所有电量。只有在切断板子电源，且大容量电容器完全放电后，才可更换待测试器件

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ボードを操作するとき、正確な安全ルールを守るのを確保すべきです。さもないと、以下の危険がある可能性があります：

- 死亡
- 重症
- 感電
- 電撃
- 電気の火傷
- 厳しい火傷

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Table of Contents

| | |
|---|-----|
| 1. Introduction..... | 7 |
| 2. Design Specifications | 8 |
| 3. Physical Dimensions and Pinouts | 10 |
| 4. System Overview | 11 |
| 4.1 Power Board | 14 |
| 4.1.1 AC-DC Power Stage | 14 |
| 4.1.2 DC-DC Power Stage | 29 |
| 4.1.3 Control Structure of the Converter | 49 |
| 4.1.4 Gate Drive Circuitry | 54 |
| 4.1.5 Design and Layout Considerations for High Frequency Switching | 59 |
| 4.2 Controller Board | 63 |
| 4.2.1 Power Supply Requirements | 64 |
| 4.2.2 Analog Feedbacks | 68 |
| 4.2.3 Controller Pin Assignments | 71 |
| 5. Performance Data | 75 |
| 6. Appexdix. | 83 |
| 7. References | 104 |
| 8. Revision History | 104 |

1. Introduction

Electric vehicle (EV) is a rapidly growing segment for transportation nowadays as the world is moving towards cleaner fuel alternatives. The battery of the EV needs to be charged while parked at home or office. While this requires only AC/DC conversion with isolation and front-end PFC, the trend is towards the bi-directionality of the converter i.e. feeding power into the grid from battery side. The main reason of the bi-directionality requirement is because the EV battery is imagined as a distributed energy storage system and may play a great part in stabilizing the grid. It may feed power into the grid when demand is at peak and vehicle is stationary and draws power from the grid when demand is low.

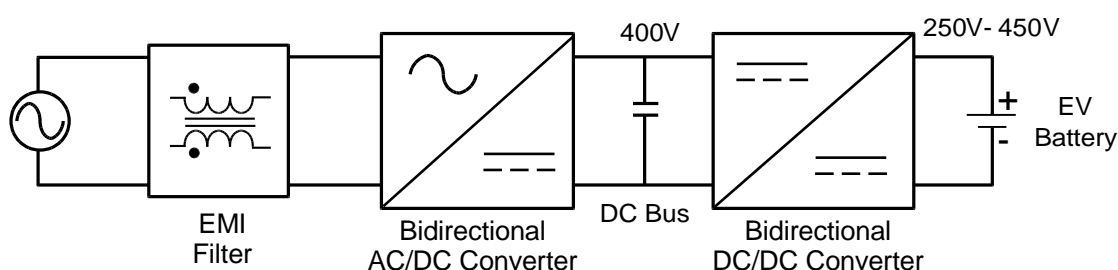


Figure 1. EV Battery Charging System

Figure 1 shows the most popular topology using conventional Si devices where intermediate DC link voltage is fixed at 400VDC. It is well known that the resonance converters are the most efficient converters due to their ability to work at the resonance frequency. The disadvantage of fixing the DC link at 400VDC is that the converter works at a frequency far more from the resonance frequency to accommodate the widely varying EV battery voltage, thus reducing the efficiency considerably.



Figure 2. Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger

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In this application note, Cree has introduced a highly efficient CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger (as shown in Figure 2) based on Cree's (C3M™) 1000V, 65mΩ (P/N: C3M0065100K) SiC MOSFET which comes in a TO-247-4 package with a Kelvin source availability. The main features of Cree's (C3M™) SiC MOSFETs include: Low switching losses, fast intrinsic body diode and high frequency operation which not only reduces the overall weight and size of the system but it also has a significant impact on the efficiency of the whole system.

Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger comprises of two power stages: 1) Bi-Directional PFC stage and 2) Isolated Bi-directional DC/DC stage (as shown in Figure 3). The Bi-Directional PFC stage is based on the Totem-Pole PFC Topology while the Isolated Bi-Directional DC/DC stage is based on a CLLC topology with a variable DC link voltage (as shown in Figure 3). At full load, the DC link voltage varies according to the variations in battery voltage and the CLLC topology operates at resonance or close to the resonance frequency. This optimizes the efficiency of the bi-directional CLLC converter (as shown in Figure 3) and its overall efficiency remain higher as compared to the fixed DC link LLC converter.

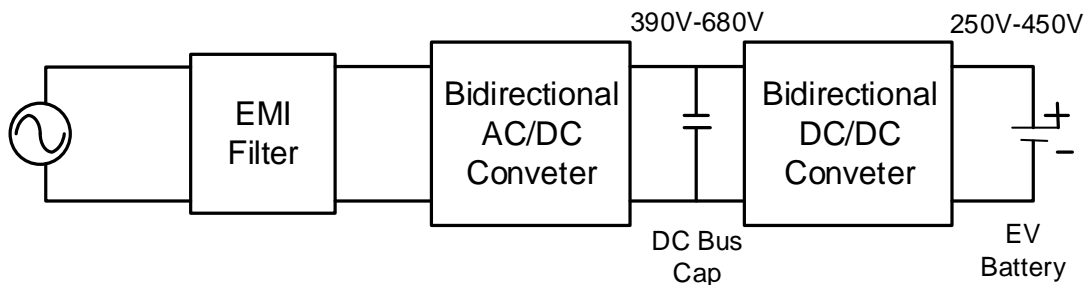


Figure 3. Bi-Directional EV Battery Charging System with Variable DC Link Voltage

2. Design Specifications

The design specifications of both charging and inversion modes of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger are listed in Table 1.

| Charging Mode | | |
|------------------------------|-------------------------------|---|
| Parameters | Values | Notes |
| Input voltage range | 90VAC-265VAC 200VAC-265VAC | Power will be limited when input voltage is below 200 VAC |
| THD and PF | THD <5% and PF > 0.99 | At Rated Power |
| Output voltage range | 250VDC-450VDC | Output current will be limited to 20A when the battery voltage is below 320VDC; Constant Power between 320VDC-430VDC; constant voltage above 430VDC |
| Input rated power | 6.6 kW | |
| Isolation voltage | > 2.5 kV | |
| Switching frequency of PFC | 67 kHz | |
| Switching frequency of DC/DC | 200 kHz | |
| Peak Efficiency | > 96% | |
| Max Ambient Temperature | 65 °C | |
| Inversion Mode | | |
| Parameters | Values | Notes |
| Input voltage range | 250VDC-450VDC | When the battery voltage is below 320VDC, it will stop delivering power |
| THD and PF | THD <5% and PF > 0.99 | At Rated Power |
| Output voltage range | 220VAC \pm 5% | |
| Input rated power | 3.3 kW | |
| Isolation voltage | > 2.5 kV | |
| Switching frequency of DC/AC | 67 kHz | |
| Switching frequency of DC/DC | 200 kHz | |
| Peak Efficiency | > 96% | |
| Max Ambient Temperature | Room Temperature | Forced air cooling for the base plate or the completed PCBA |

Table 1: Design Specifications of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger

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3. Physical Dimensions and Pinouts

The Physical dimensions and the pinouts of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger has been shown in Figure 4(a) and Figure 4(b).

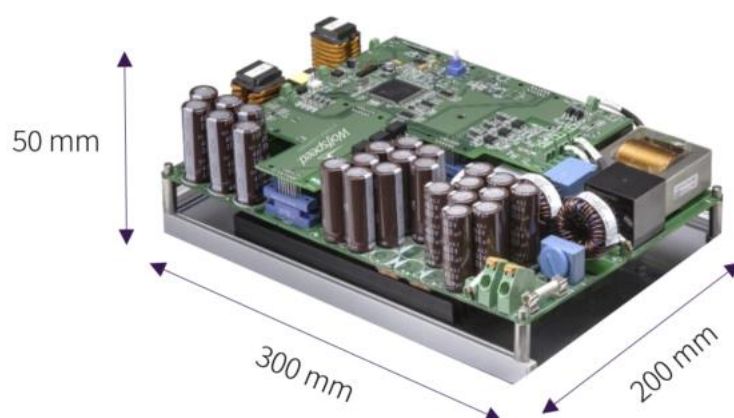


Figure 4 (a)

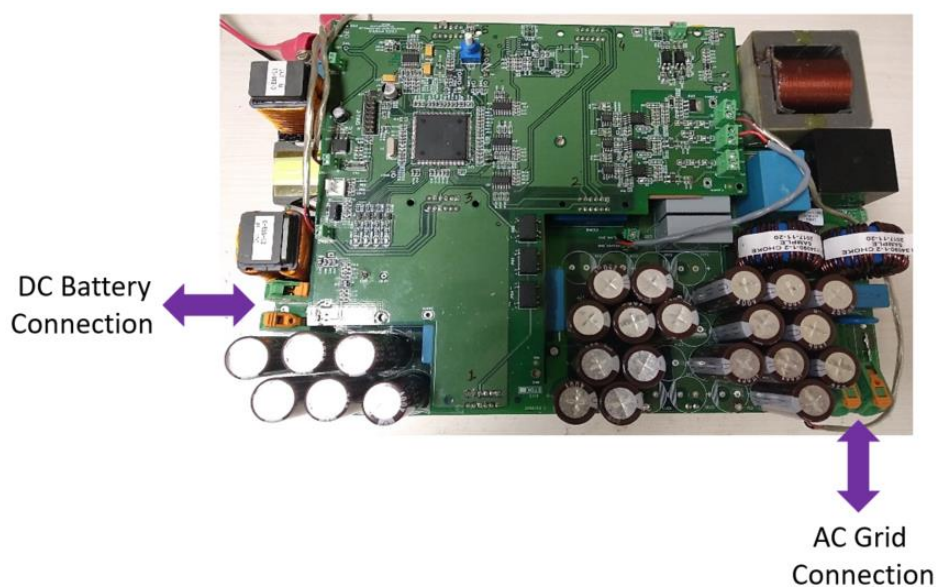


Figure 4 (b)

Figure 4(a). Physical Dimensions of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger

Figure 4(b). Pinouts of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger

4. System Overview



CAUTION

HIGH VOLTAGE RISK

THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS BOARD WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS BOARD CAN REACH TEMPERATURES ABOVE 50° CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED. DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD.

The connectors on the board have very high voltage levels present when the board is connected to an electrical source, and thereafter until the bulk capacitors are fully discharged. Please ensure that appropriate safety procedures are followed when working with these connectors as serious injury, including death by electrocution or serious injury by electrical shock or electrical burns, can occur if you do not follow proper safety precautions. When devices are being attached for testing, the board must be disconnected from the electrical source and all bulk capacitors must be fully discharged. After use the board should immediately be disconnected from the electrical source. After disconnection any stored up charge in the bulk capacitors will continue to charge the connectors. Therefore, you must always ensure that all bulk capacitors have completely discharged prior to handling the board.

警告

高压危险

接通电源后，该评估板上可能存在非常高的电压，板子上一些组件的温度可能超过 50 摄氏度。此外，移除电源后，上述情况可能会短暂持续，直至大容量电容器完全释放电量。通电时禁止触摸板子，应在大容量电容器完全释放电量后，再触摸板子。

板子上的连接器在充电时以及充电后都具有非常高的电压，直至大容量电容器完全释放电量。请确保在操作板子时已经遵守了正确的安全流程，否则可能会造成严重伤害，包括触电死亡、电击伤害或电灼伤。连接器件进行测试时，必须切断板子电源，且大容量电容器必须释放了所有电量。使用后应立即切断板子电源。切断电源后，大容量电容器中存储的电量会继续输入至连接器中。因此，必须始终在操作板子前，确保大容量电容器已完全释放电量。

警告

高压危险

通电してから、ボードにひどく高い電圧が存在している可能性があります。ボードのモジュールの温度は50度以上になるかもしれません。また、電源を切った後、上記の状況がしばらく持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。通电している時にボードに接触するのは禁止で

す。大容量のコンデンサーで電力をまだ完全に釈放していない時、ボードに接触しないでください。ボードのコネクターは充電中また充電した後、ひどく高い電圧が存在しているので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。ボードを操作している時、正確な安全ルールを守っているのを確保してください。さもないければ、感電、電撃、厳しい火傷などの死傷が出る可能性があります。設備をつないで試験する時、必ずボードの電源を切ってください。また、大容量のコンデンサーで電力を完全に釈放してください。使用后、すぐにボードの電源を切ってください。電源を切った後、大容量のコンデンサーに貯蓄している電量はコネクターに持続的に入るので、ボードを操作する前に、必ず大容量のコンデンサーの電力を完全に釈放するのを確保してください

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The block diagram of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger is shown in Figure 5. The system designed in the lab does not have a battery charging algorithm built in and customer may code their own battery charging algorithm in the DSP.

The ac-dc converter stage is configured as a totem pole PFC circuit in charging mode. The circuit has two half bridge circuits; one switching at high frequency of 67kHz and the other at the frequency of grid voltage, typically 50Hz. Both legs of the PFC circuit consist of two of the Cree's 1000V, 65mΩ SiC MOSFETs (C3M0065100K) in a parallel arrangement. The DC-DC bi-directional CLLC converter comprises of 2 identical H-bridges separated by isolation transformer. A resonance frequency of 200kHz was selected for the optimum operation. All switches have isolated gate drivers with a separate isolated power supply. Ceramic de-coupling capacitors in proximity with small film capacitors have been used for the decoupling of the stray inductances.

Larger film capacitors have been used a little farther away from the devices for high frequency ripple current. A bank of electrolytic capacitors has been connected in series with DC link due to the availability of 680V DC link voltage.

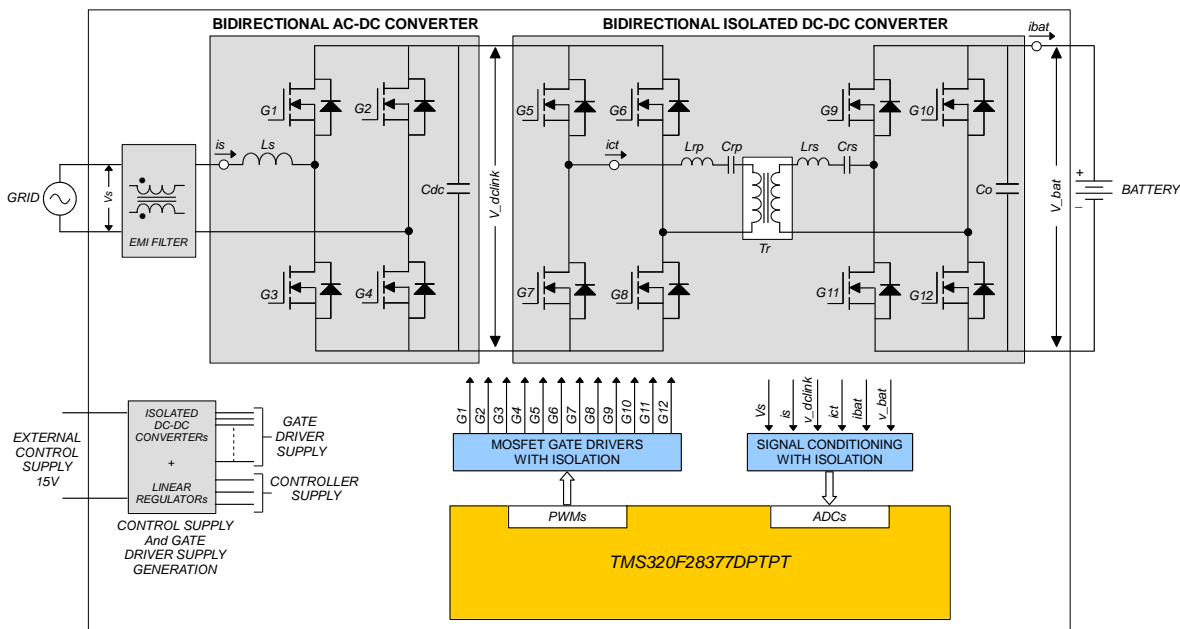


Figure 5. System Level Block Diagram of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger

The control card is based on Texas Instruments (TI) DSP controller (P/N: TMS320F28377). Controller card is galvanically isolated from the power stage through isolated gate drivers, analog isolation amplifiers and the opto-isolators. For controller supply and driver supply, external isolated power supplies of 7V and 15V are connected to the control card.

4.1 Power Board

The power board of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger houses the input EMI filter and the power stages of both AC-DC and DC-DC converters. The controller board is placed in such a way that the PWM signals of each power stage remain as close as possible to the respective gate driver. The gate drive circuitry has also been placed close to the respective SiC MOSFETs. To do the test measurements, the DC and AC voltages and currents are routed to the controller through separate connectors. The external power supply of the gate drivers is also routed through the controller board.

4.1.1 AC-DC Power Stage

The AC-DC converter is a H-bridge circuit with bidirectional power transfer capability. In charging mode, the converter is configured as totem pole PFC boost converter, as shown in Figure 6 and operates as a sinewave inverter with hybrid modulation (or modified unipolar modulation) in inversion mode. One leg of the converter is switched at low frequency (at grid frequency or the reference sinewave frequency) while the other leg is operated at high frequency. The EMI filter is designed to minimize the conducted emission noise to the grid and keep it to level well below the standards.

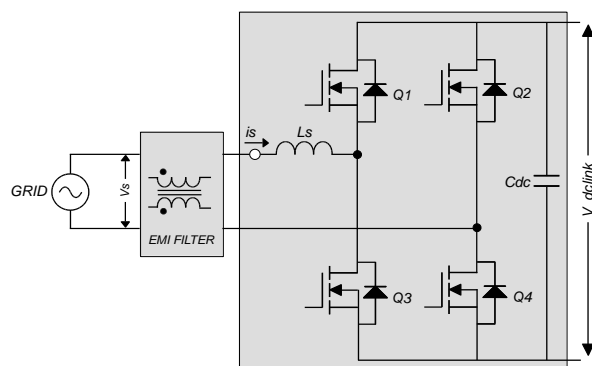


Figure 6: AC-DC Converter Power Stage

In the charging mode, the AC-DC converter stage should regulate the DC bus voltage as well as maintain a good THD in the grid current. Without any switching, the body diodes of MOSFETs will create a full bridge uncontrolled rectifier circuit and current drawn from grid will be pulsating in nature. With a proper switching sequence and two loop control mechanism, the DC bus is regulated to the required DC voltage while maintaining the inductor current close to sinusoidal shape and in phase with the grid voltage.

The gate pulses of MOSFETs Q2 and Q4 are complementary and change their state based on the zero crossing of the grid voltage. For the positive half of the grid voltage, Q4 gate signal set as high while Q2 gate signal set as low. MOSFET Q3 is switched at high frequency with varying pulse widths based on the current loop compensator and the output of the control logic. For the negative half of the grid voltage, MOSFETs Q4 and Q2 switch their states while MOSFETs Q3 and Q1 switch their functionalities. The resultant configuration is a boost converter circuit for each half of the AC cycle (as shown in Figure 7). The schematic on the left side of the Figure 7 depicts the switching states for the positive half cycle and the schematic on the right side of the Figure 7 depicts the switching states for the negative half cycle. The blue line indicates the switching state when the current in boost inductor raises and the load is supported by the output capacitors. The red line indicates the switching state when input voltage along with the inductor energy feed the load and the capacitor at higher voltage.

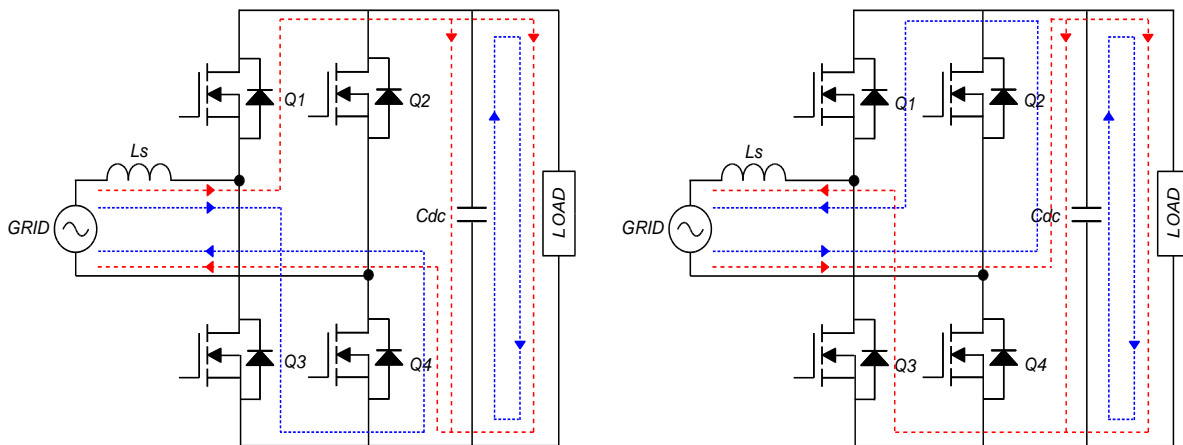


Figure 7. Totem-Pole PFC Current Path for Positive Half Cycle (Left) and Negative Half Cycle (Right)

In the inversion mode, the circuit is configured to work as a grid tie inverter and feed the grid from the available battery energy. The switching scheme remains the same as it has been followed in the totem pole PFC while the grid current is controlled to be in phase with the voltage.

| Parameters | Values | Notes |
|--------------------------|-----------------------|--|
| Grid Voltage Range | 90VAC-265VAC | Power will be limited when input voltage is below 200 VAC |
| THD and PF | THD <5% and PF > 0.99 | At Rated Power (Both Modes) |
| DC Bus Voltage Range (1) | 390VDC - 680VDC | AC-DC Mode |
| DC Bus Voltage Range (2) | 480VDC - 680VDC | DC-AC Mode |
| Output Power (1) | 6.6 kW | AC-DC Mode: $V_{Grid} = 200 \text{ VAC to } 265 \text{ VAC}$ |
| Output Power (2) | 3.3 kW | DC-AC Mode |
| Switching Frequency | 67kHz | |
| Converter Efficiency | > 98% | |

Table 2. Specifications of the AC-DC Stage

Inductor Design:

Referring to the specifications in Table 1, the maximum power to be handled is in charging mode. So, the inductor is designed for totem-pole PFC converter with continuous conduction mode. The input voltage is sinusoidally varying in a boost PFC converter and the ripple current in the inductor will not be constant for a known power value. The inductor current ripple (Δi_L) is given by:

$$\Delta i_L = \frac{v_{in}(V_o - v_{in})}{F_s L V_o}$$

For a maximum inductor ripple current of 15A (approximately 35%), at 200VAC input (283V peak) and at maximum DC output (670V), the required inductance value (L) would be:

$$L = \frac{v_{in}(V_o - v_{in})}{F_s V_o \Delta i_{L(max)}} = \frac{283 \times (680 - 283)}{67000 \times 670 \times 15} = 166.8 \mu H$$

The maximum ripple current $\Delta i_{L(\max)}$ in the inductor (L) when the input voltage $v_{in} = \frac{V_o}{2}$:

$$\Delta i_{L(\max)} = \frac{V_o}{4F_s L}$$

The maximum inductor current ripple ($\Delta i_{L(\max)}$) will be 15.2A when output (V_o) is set at 680V DC and instantaneous input voltage ($V_{in(ims)}$) is 340V.

In the Inverter mode, the input (v_{in}) to the converter is a fixed DC bus voltage and the output (V_o) is a sinusoidal AC voltage. The converter should be in continuous conduction mode to keep the switching harmonics in grid current at the minimum level. The required value of inductance (L) in the Inverter mode with a 3A ripple current (Δi_L) (approximately 32% ripple) is:

$$L = \frac{(V_{dc} - V_{opk})V_{opk}}{V_{dc} F_s \Delta i_{L(\max)}} = \frac{(390 - 325) \times 325}{390 \times 67000 \times 3} = 303\mu H$$

| Charging Mode | | |
|----------------|--------|-------------------------------------|
| Parameters | Values | Notes |
| Inductance | 165μH | At maximum Input AC Current of 33 A |
| RMS Current | 33A | For 6.6 kW Power at 200 V |
| Peak Current | 54A | |
| Ripple Current | 15A | At 67 kHz |
| Inversion Mode | | |
| Parameters | Values | Notes |
| Inductance | 300μH | At maximum Input AC Current of 33 A |
| RMS Current | 14A | For 3.3 kW Power at 230 V |
| Peak Current | 15.5A | |
| Ripple Current | 3A | At 67 kHz |

Table 3. Inductor Requirements

$$I_{inmax_{rms}} = 34.375A$$

$$I_{inmax_{pk}} = 48.6A$$

$$I_{ripple_{pkpk}} = 0.4 * I_{inmax_{pk}} = 19.4425$$

$$I_{boost_{pk}} = I_{inmax_{pk}} + \frac{I_{ripple_{pkpk}}}{2} = 58.312$$

$$D_{min} = 1 - \frac{(\sqrt{2} * V_{inmin_{rms}})}{V_{opfc}} = 0.411$$

When the boost inductor has 24.613A DC bias current, the inductance will be:

$$L_{boost_{bias}} = \frac{(\sqrt{2} * V_{inmin_{rms}} * D_{min})}{(F_{s_{pfc}} * I_{ripple_{pkpk}})} = 132.82\mu H$$

$$\text{Area Product required} = AeAw_{required} = \frac{L_{boost_{bias}} * I_{boost_{pk}}^2}{Kw_{boost} * B_{max_{boost}} * J_{max_{boost}}}$$

$$B_{max_{boost}} = 0.5T$$

$$J_{max_{boost}} = 750 \frac{amp}{cm^2}$$

$$AeAw_{required} = 1.72 * 10^{-7} m^4$$

An available core with part number: APH46P60 has been selected. The details of APH46P60 has been shown in Figure 8.

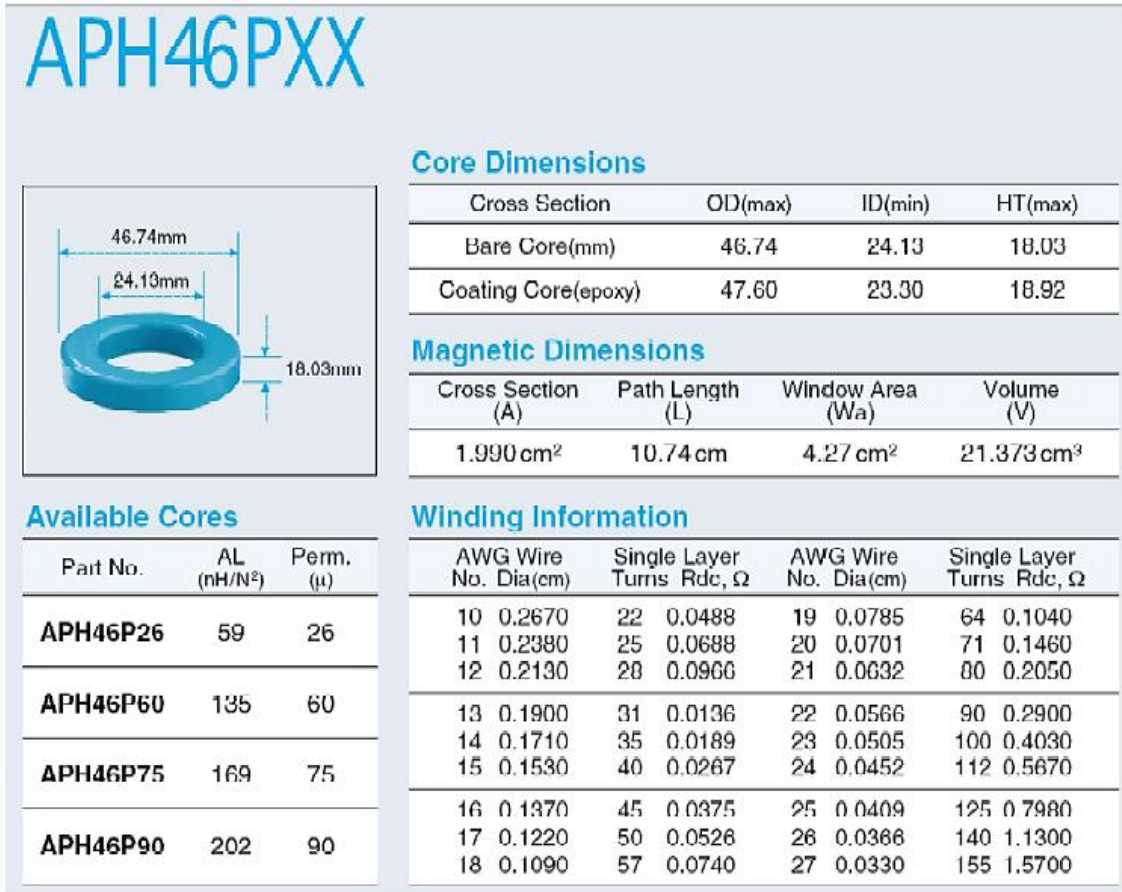


Figure 8. Core Details of APH46P60

Considering 2 cores stacked AeAW of selected inductor (L):

$$L = 2 \cdot 1.99 \cdot 4.27 \cdot 10^{-8} = 1.699 \cdot 10^{-7} \text{ m}^4$$

Inductance factor value of 2 cores stacked $AL_N = 2 \cdot 0.135 \mu\text{H} = 0.27 \mu\text{H}$

$$N_{boost} = 2 \cdot \sqrt{\frac{L_{boost_{bias}}}{AL_N}} = 44.35$$

$$L_{boost_{nobias}} = 531.285 \mu\text{H}$$

$$H_{boost_{max}} = N_{boost} * \frac{(I_{inmax_{pk}} + \frac{L_{boost_{bias}} * I_{ripple_{pk2pk}}}{2 * L_{boost_{nobias}}})}{le}$$

$$H_{boost_{max}} = 264.822$$

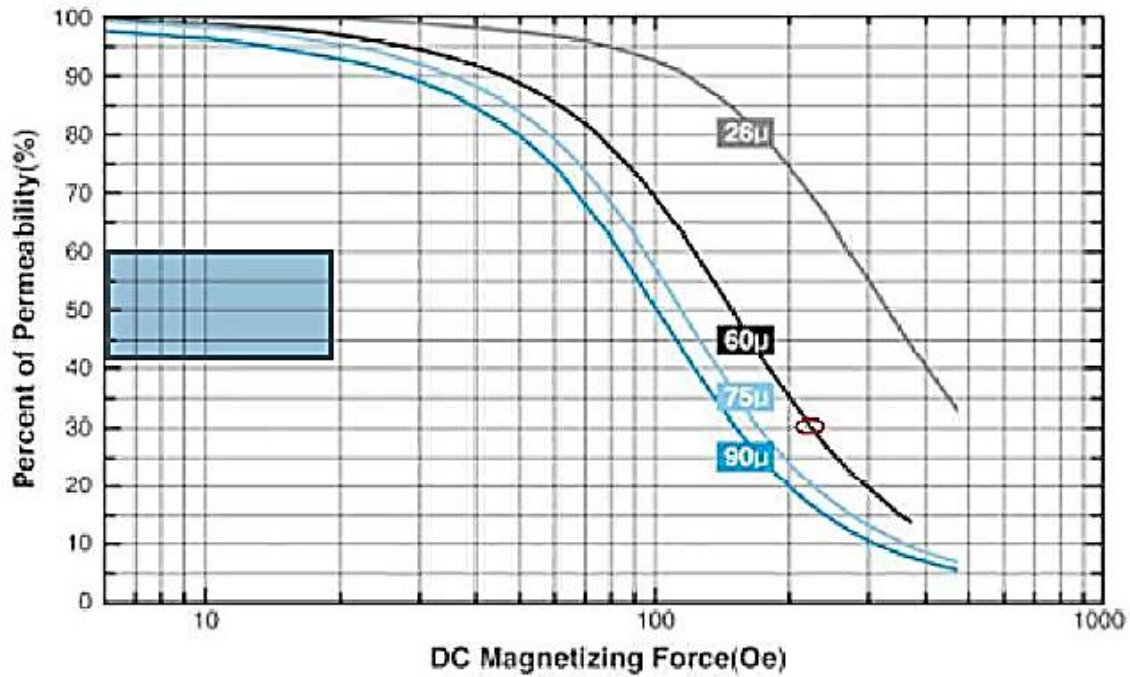


Figure 9. % Permeability Vs DC Magnetizing Force of APH46P60

The permeability with DC bias curve shows about 30% initial permeability at:

$$H_{boost_{max}} = 264.822 \text{ oersteds for } 60\mu \text{ material.}$$

The inductance with $H_{boost_{max}} = 264.822$ dc bias

$$L_{boost_{bias}} = 0.3 * L_{boost_{nobias}} = 159.385\mu\text{H.}$$

For winding 2*1.4mm wire is used and total DC resistance = 14mΩ

DC Bus Capacitor Selection

DC Bus capacitor selection depends on the capacitor's capability of withstanding the entire output voltage range, minimize the switching ripple as well as low frequency ripple and hold sufficient energy to support the load in an event of power outage for at least one cycle. This results in three criteria for capacitor selection.

$$C_o > \frac{P_o}{2\pi F_{grid} V_o \Delta V_o} \approx 1.5mF \text{ for 20V line frequency ripple}$$

$$C_o > \frac{2P_o t_{hold}}{V_{omax}^2 - V_{omin}^2}$$

$$\approx 890\mu F \text{ to hold 6.6kW power for 20ms}$$

In inverter mode, the same criteria hold good for DC bus capacitor selection. Since the power to be pumped to the grid is 3.3kW, capacitors designed for charging mode are sufficient for the inverter mode.

The maximum of the three values (i.e. 1.5mF) is the required capacitance which satisfies the switching ripple requirement. Cree has allowed slightly higher ripple here and selected a value of 1.1mF instead of 1.5mf. Hold up criteria does not apply here. The RMS current that the capacitor needs to handle is:

$$I_{Co,rms} = \sqrt{\frac{8\sqrt{2} P_o^2}{3\pi V_{acmin} V_o} - \frac{P_o^2}{V_o^2}}$$

The ripple current rating corresponds to the line frequency component in the capacitor current and it can be evaluated at the minimum AC voltage for which rated power is to be supported.

$$I_{Co,rms} = \sqrt{\frac{8\sqrt{2} \times 6600^2}{3\pi \times 200 \times 680} - \frac{6600^2}{680^2}} = 17 A$$

To cater the requirements of large operating voltage range and high ripple current along with the need for longer operating life, a capacitor bank made of electrolytic capacitors is used. The details

of the capacitor bank are listed in Table 4. Apart the DC Bus capacitor, several low value snubber capacitors close to the devices and couple of low value film capacitors have been used as well to minimize switching noise in the DC bus.

| Parameters | Values | Notes |
|--------------------------------------|------------------------------|---|
| Capacitor used | EKXJ401ELL251MM50S | From Chemi-Con |
| Capacitor rating | 250 μ F, 400VDC | |
| Series parallel combination | 2 in series 9 in parallel | Series connection for voltage and parallel connection for ripple current rating |
| Capacitor bank rating | 1.125mF 800VDC | |
| Capacitor bank ESR | 0.044 Ω | At 105°C and 120Hz ripple |
| Capacitor bank ripple current rating | 17.71A | At 105°C and 120Hz ripple |
| Capacitor bank life | | At 105°C with ripple |
| Operating temperature range | -40°C to +105°C | |

Table 1. Dc Bus Capacitor Bank specifications

When the converters are not operational, the DC bus is charged to the peak of the grid voltage of 375V. The individual capacitors are rated at 400V and the capacitor bank can withstand the maximum grid voltage without the need of a voltage balancing circuit.

Soft Charging of DC bus Capacitors:

When the grid is connected to the charger, the body diodes of PFC stage MOSFETs act as a single phase full bridge rectifier with a large capacitor filter at the DC Bus. The uncharged capacitors, equivalent to a short-circuited path, draw high current from the grid till they become fully charged to the peak grid voltage. This hard charging of DC Bus capacitors can damage the body diodes of the PFC stage MOSFETs.

The peak current that the body diodes of the MOSFETs can withstand is high pulsed current for few microseconds duration, to avoid the current through the body diode for a long duration of time, a diode bridge of sufficiently large rating is connected in parallel. A small resistor to limit the inrush current is sufficient but it should have large pulsed power handling capability. Two

220Ω resistors have been placed in series with the input lines of the AC-DC stage. The maximum current limited by the resistors is:

$$I_{inpk} = \frac{V_{acinmax}\sqrt{2}}{R_{ch}} = \frac{265\sqrt{2}}{\frac{220}{2}} = 3.43 A$$

The instantaneous power dissipation in charging resistor is around 1.29kW which is according to the repetitive pulsed power dissipation rating of the rated capacitor.

MOSFET and Diode Requirements:

Referring to the specifications in Table 2, the MOSFETs and the diodes must be rated according to the maximum power handling capability of the charger mode. Apart from voltage and current ratings, the losses in the semiconductor devices need to be considered for the device selection as well.

The low frequency switching leg contributes to the conduction losses only. Though the body diodes are sufficient for PFC action, their voltage drop is large and switching the corresponding MOSFETs minimizes the conduction losses. On the high frequency leg, one MOSFET contributes to conduction and switching losses. The conduction of body diode of other MOSFET is bypassed through synchronous switching causing zero switching loss in MOSFET and zero conduction loss in body diode. The maximum voltage and current that the MOSFET should withstand is

$$V_{SWpk} = V_{omax} = 680V$$

$$I_{SWpk} = I_{Lmax} + \frac{\Delta I_L}{2} = \frac{6600}{200}\sqrt{2} + \frac{15}{2} = 54.17A$$

The currents in all the four MOSFETs are different, as Q2 and Q4 carrying non-pulsating currents (bypassing current in their body diodes) for only one half of the AC cycle (as shown in Figure 10). There is an average current which is equal to the instantaneous grid current and an input voltage dependent ripple current, both are combined in the Q2 current waveform for one half of AC cycle.

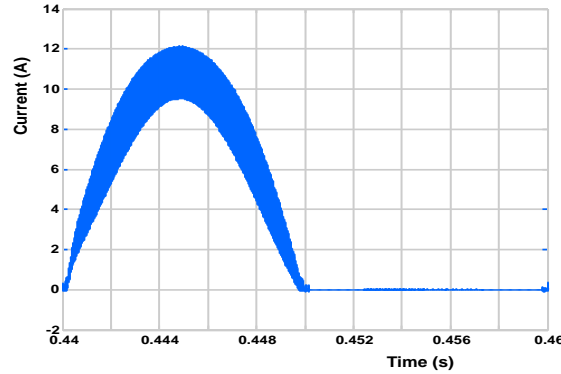


Figure 10. Current through MOSFET Q2 (or Q4)

The RMS value of MOSFET current in one switching cycle is:

$$i_{Q2rms}(\theta) = \sqrt{\left(i_{Q2avg}(\theta)\right)^2 + \frac{(\Delta i_L(\theta))^2}{12}}$$

For continuous conduction mode of operation, the RMS quantity due to the ripple current is:

$$i_{Q2rms}(\theta) \approx \sqrt{\left(i_{Q2avg}(\theta)\right)^2} = \sqrt{\left(\frac{\sqrt{2} P_{in}}{V_{inrms}} \sin(\theta)\right)^2}$$

The RMS value of MOSFET current over one cycle of line voltage is:

$$I_{Q2rms} = \sqrt{\frac{1}{2\pi} \int_0^\pi \left(i_{Q2rms}(\theta)\right)^2 d\theta} = \frac{P_{in}}{\sqrt{2} V_{inrms}}$$

The full load is to be supported for grid voltage up to 200V. The maximum RMS current stress on MOSFETs Q2 and Q4 is:

$$I_{Q2rms} = I_{Q4rms} = \frac{6600}{\sqrt{2} \times 200} = 23.34A$$

The MOSFETs on the high frequency leg are operating like boost converter with synchronous rectification. The current waveform through MOSFET (Q3) is illustrated in Figure 11, neglecting the inductor ripple current slope for continuous conduction mode.

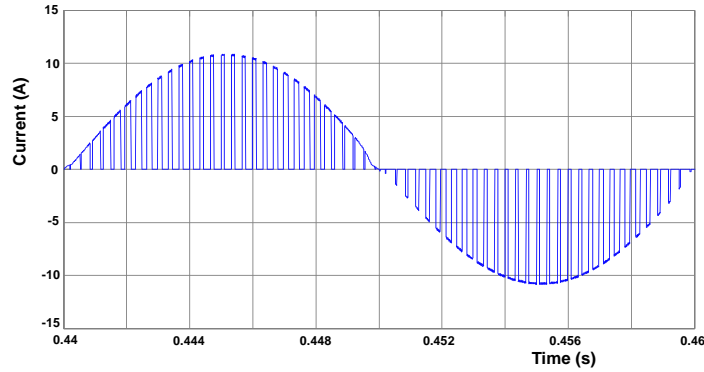


Figure 11. Current through MOSFET Q3

For the positive half cycle of AC voltage, MOSFET current is from drain to source and for the negative half cycle, the body diode current is by passed through the MOSFET. The RMS current of MOSFET Q3 for each half cycle is:

$$i_{Q3rms+}(\theta) = \frac{\sqrt{2} P_{in}}{V_{inrms}} \sin(\theta) \sqrt{1 - \frac{\sqrt{2} V_{inrms} \sin(\theta)}{V_o}} \text{ for } 0 \leq \theta \leq \pi$$

$$i_{Q3rms-}(\theta) = \frac{\sqrt{2} P_{in}}{V_{inrms}} |\sin(\theta)| \sqrt{\frac{\sqrt{2} V_{inrms} (-\sin(\theta))}{V_o}} \text{ for } \pi < \theta \leq 2\pi$$

The RMS current of MOSFET Q3 for one full cycle of grid voltage is:

$$I_{Q3rms} = \sqrt{\frac{1}{2\pi} \left(\int_0^\pi (i_{Q3rms+}(\theta))^2 d\theta + \int_\pi^{2\pi} (i_{Q3rms-}(\theta))^2 d\theta \right)}$$

$$I_{Q3rms} = I_{Q1rms} = \frac{P_{in}}{\sqrt{2} V_{inrms}} = \frac{6600}{\sqrt{2} \times 200} = 23.34A$$

Power Loss Estimation:

The power loss in the AC-DC stage occurs in all four MOSFETs, the boost inductor and the input EMI filters. Other losses in the trace resistances can be neglected. The worst-case loss numbers

can be obtained at rated power (6.6kW) for the minimum input voltage (200VRMS) and the maximum output voltage (680V DC).

1. Conduction Losses in the Boost Inductor: The maximum possible conduction loss in the main inductor of the AC-DC stage is (using the dc resistance value from datasheet):

$$P_{inductor} = \left(\frac{P_{in}}{V_{inrms}} \right)^2 0.0113 = \left(\frac{6600}{200} \right)^2 0.0145 = 15.8 \text{ W}$$

$$P_{core} = 19W \text{ at } 680V \text{ DC link}$$

2. Conduction Losses in MOSFETs: Two MOSFETs are in parallel position for each switch of the AC-DC converter and the synchronous rectification is enabled for minimizing losses in the body diodes. The RMS currents of both high and low frequency switching MOSFETs are the same. The Rds(on) of SiC MOSFETs depend on the gate voltage and the junction temperature as shown in Figure 12. The variation of Rds(on) with the operating current is not large and can be assumed constant.

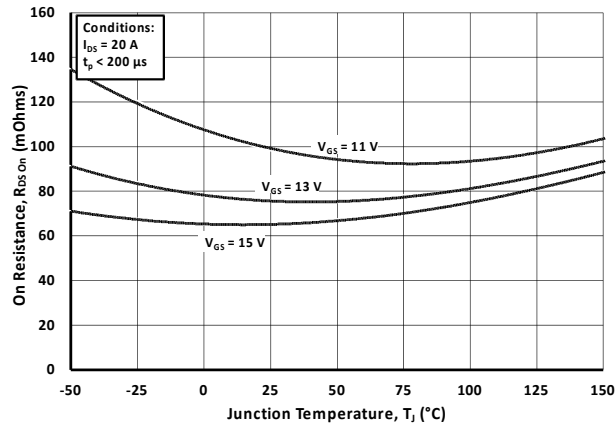


Figure 12. C3M0065100K Rds(on) vs temperature for various gate voltage

From Figure 12, the Rds(on) of MOSFET is approximately 75mΩ for the gate voltage of 15V at the junction temperature of 150°C. The conduction losses in each MOSFET pair is:

$$P_{CD-mosfet} = 2 \left(\frac{I_{Q1rms}}{2} \right)^2 0.075 = \left(\frac{23.34}{2} \right)^2 0.075 = 20.42 \text{ W}$$

4. Switching Losses in MOSFETs: The switching losses in the MOSFETs Q2 and Q4 can be ignored as they are switching at the grid voltage frequency. Also, the reverse recovery losses for these two MOSFETs can be ignored. The switching losses come into play for MOSFETs Q1 and Q3 as they are switching at 67kHz. When one of those MOSFETs starts switching as a synchronous rectifier, the body diode turned ON first followed by the MOSFET resulting in ZVS. However, the reverse recovery of the body diode will cause switching losses when the other switch turned on. When MOSFETs Q1 or Q3 starts switching as a main boost converter switch, they must dissipate both turn ON and turn OFF losses.

The switching energies for SiC MOSFETs are dependent on the gate resistance and the drain current as shown in Figure 13. The switching energy variation on junction temperature is minimum. For MOSFET Q3, the ON/OFF current in positive half cycle is varying as shown in

Figure 11 and so does the switching losses. In the negative half cycle, the switching losses indicates the diode recovery losses:

$$P_{SW-Q3} = \frac{1}{2\pi} \left(\int_0^\pi F_s (e_{ON}(\theta) + e_{OFF}(\theta)) d\theta + \int_\pi^{2\pi} \frac{1}{2} F_s Q_{rr} U_{dd} d\theta \right)$$

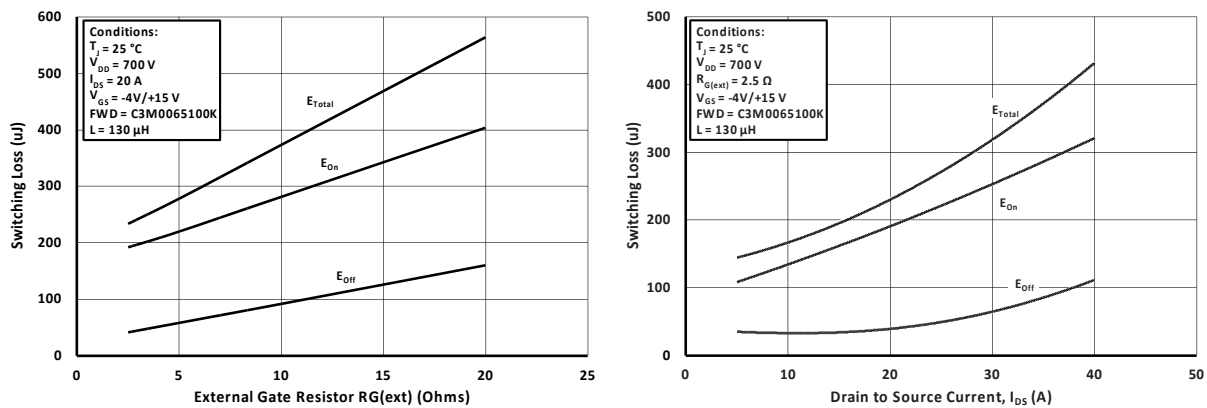


Figure 13. Cree's C3M0065100K, Switching Energy Vs Drain Current (Right) and Switching Energy Vs Gate Resistance at 700V (Left)

The turn ON and turn OFF losses are the functions of instantaneous drain current as shown in Figure 13. The switching loss profile for MOSFET Q1 over one AC cycle is shown in Figure 14 (for the worst-case conditions described for conduction loss calculations). The average switching loss over one AC cycle is computed to be 14.56W per switch pair.

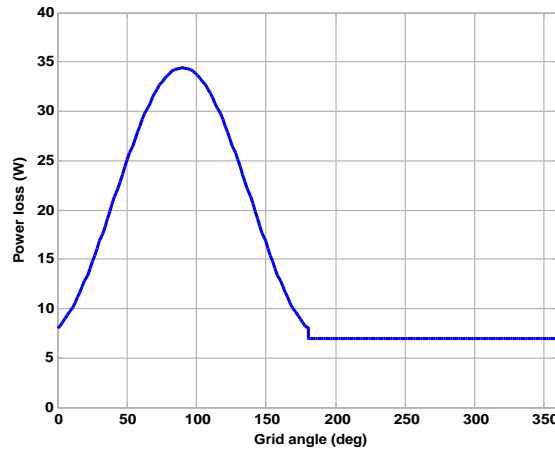


Figure 14. Switching loss for Q1 over one AC cycle

The total losses in the AC-DC stage are:

$$P_{ac-dc\ loss} = (4 \times P_{CD-mosfet}) + (2 \times P_{SW-Q3}) + P_{inductor}$$

$$P_{ac-dc\ loss} = 126.6\ W$$

4.1.2 DC-DC Power Stage

For the DC-DC converter stage, the input voltage is taken from the output of the AC-DC stage. The range of this input voltage is from 390 VDC to 680 VDC with an additional superimposed ripple of 26V. The ripple frequency is approximately equal to the double of the line frequency. The output of the DC-DC power stage is connected to the battery that has an availability of wide voltage range (250VDC-450VDC). Galvanic isolation is also required between AC and the battery side from safety point of view. The common topology for isolated DC-DC converter is the phase shifted full bridge topology with a constant switching frequency. Some issues with this topology includes: ZVS in the primary switches occur for a small range of load, higher leakage inductance in the form of external inductance is required to achieve ZVS for larger loads which results in duty cycle loss, for higher battery voltage applications, the turn OFF voltage spike in the secondary switches is higher which further increase overall losses or designer need to utilize snubbers or active clamp circuits, high losses and EMI issues for high voltage applications do not allow the use of constant frequency full bridge converters. Dual active bridge (DAB) options were also explored for DC/DC stage but were not found very suitable. Simulation studies showed that CLLC converter with its bi-directional property was most suited for this application. Resonant converters are better choice to achieve low EMI in high input output voltage cases as well.

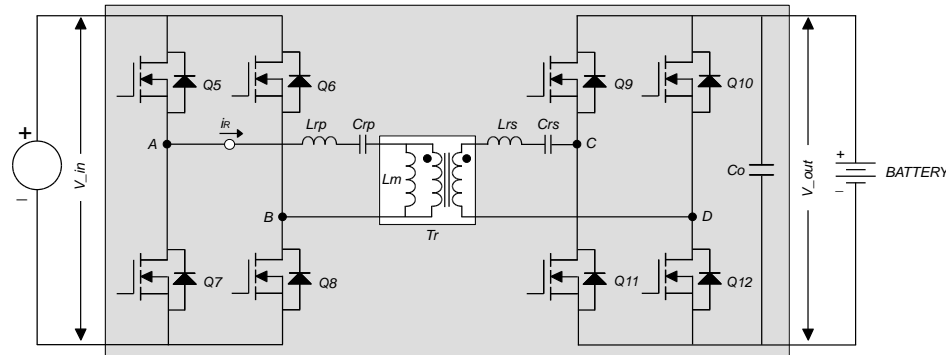


Figure 15. Bidirectional CLLC resonant converter power stage

The DC-DC converter stage is a bidirectional resonant converter or a CLLC converter as shown in Figure 15. This converter is similar to the conventional LLC with an additional LC pair on the secondary side. For a wide output voltage range, LLC resonant converter is suitable since ZVS occurs at turn ON for all the switches, leakage inductance is a part of resonance action and resonance frequency can be kept higher to reduce size of the converter.

It is well known that LLC resonance converter is most efficient when it operates at resonance frequency. At resonance frequency, turn OFF current is equal to the magnetizing current and circulating energy is smaller. Magnetizing inductance can be designed to be of optimum value from loss point of view because frequency vs gain characteristic is not required. Some of the advantages are of course compromised because the PFC inductor is not optimized and leads to higher losses at higher DC link voltage. Still, compared to variable resonance frequency operation, it leads to higher overall efficiency. Thus DC-DC stage has been designed to operate at resonance frequency of operation. It means that the DC link voltage varies in response to the battery voltage and current.

Referring to Figure 16, L_{rp} , L_{rs} (combined with leakage inductance) and L_m along with C_{rp} and C_{rs} form a part of resonance network. In battery charging mode, MOSFETs Q5 to Q8 form a full bridge work as quasi square wave generator whereas the body diodes of Q9 to Q12 act as rectifiers and vice versa in the inverter mode. The magnetizing inductance L_m is a part of transformer T_r , which provides galvanic isolation between battery and the grid. The power stage specifications of the DC-DC stage have been shown in Table 5.

| Parameters | Values | Notes |
|-----------------------|-------------|--|
| DC bus voltage range | 390V – 680V | AC-DC Mode |
| | 480V-680V | DC-AC Mode |
| Battery voltage range | 250V – 450V | AC-DC Mode |
| | 320-450V | DC-DC Mode |
| Output power | 6.6kW | AC-DC Mode: For battery voltage range of 250V to 450V and grid voltage of 200V |
| | 3.3kW | DC-AC Mode |
| Isolation voltage | > 2.5kV | In both modes for any operating condition |
| Resonance frequency | 200 kHz | |
| Converter efficiency | > 98% | |

Table 5. Specifications of DC-DC Stage

Converter Analysis and Operation:

The equivalent model for the resonant converter in charging mode is shown in the top portion of Figure 161. The primary side bridge output v_{AB} is a square wave with peak magnitude as of input voltage and switching frequency of F_s . The circuit is in resonance in most of the cases and the current i_p will be sinusoidal. Thus, the voltage v_{AB} can also be assumed to be sinusoidal with fundamental voltage responsible for power transfer. The load resistance can be shifted to the rectifier input and all the components when referred to transformer primary yield a first harmonic approximation (FAH) circuit as shown in lower half of Figure 161e 16.

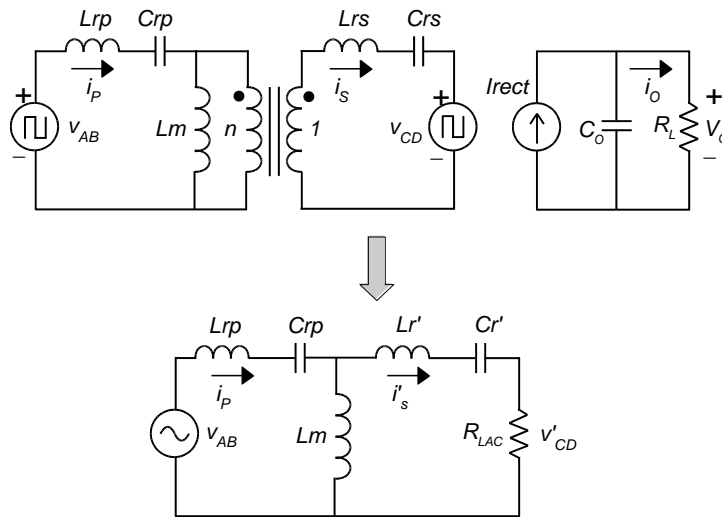


Figure 161. Equivalent circuit (Top) and FHA model of resonant converter (Bottom)

The approximated sinusoidal voltage of the FHA model is:

$$v_{AB} = \frac{4 V_{in}}{\pi} \sin(2\pi F_s t)$$

The resonant elements and load referred to primary are:

$$L_r' = n^2 L_{rs}; \quad C_r' = \frac{C_{rs}}{n^2}$$

$$R_{LAC} = n^2 \frac{8}{\pi^2} R_L$$

The load side parameters are:

$$I_O = \frac{2n}{\pi} \sqrt{2} I'_s$$

$$V_O = I_O R_L$$

From the FHA model, the converter transfer function to evaluate gain is derived as:

$$\frac{v_{CD}(s)}{v_{AB}(s)} = \frac{Z_m R_{LAC}}{Z_1 Z_2 + Z_1 (R_{LAC} + Z_m) + Z_m (R_{LAC} + Z_2)}$$

Where

$$Z_m = sL_m$$

$$Z_1 = sL_{rp} + \frac{1}{sC_{rp}}$$

$$Z_2 = sL_r' + \frac{1}{sC_r'}$$

The voltage gain curve for different frequencies at unity transformer ratio are shown in Figure 17. The gain of the converter is unity at primary side series resonant frequency and that is the desired operating point under normal operating condition. For switching frequency higher than resonance frequency, the gain is less than unity and vice-versa.

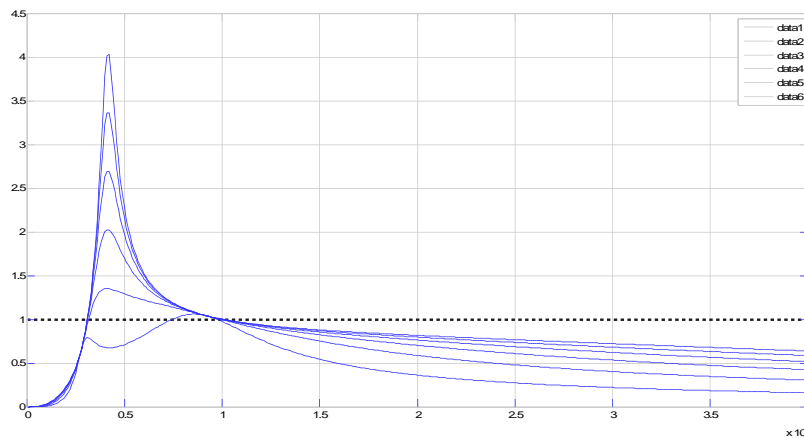


Figure 17. Voltage gain versus operating frequency for different loads

Converter Operation:

This converter operates at the resonance frequency which is decided by resonance elements of primary and secondary side. The gain for this converter is thus always unity. Though the converter can operate at below or above resonance frequency if required. This happens during starting when the converter starts at 300KHz and slowly comes to 200KHz to avoid inrush current in output capacitors. The primary side MOSFETs turn ON at zero voltage and turn OFF at small current which is equal to the magnetizing current of the transformer at resonance frequency. Secondary MOSFETs turn ON and turn OFF at zero voltage because the body diode of the corresponding MOSFET turns ON before a gate signal is given to the MOSFET.

Low reverse recovery Body diode characteristic of SiC diode are thus fully utilized here. In case of silicon MOSFET, synchronous operation of body diode may not be possible at this frequency because of large recovery time required. It is to be noted that very small voltage across body diode is available for reverse recovery and in phase shifted full bridge topology, failures have been reported due to this while using Si MOSFET. The major converter waveforms are shown in Figure 18 with six operating modes for a standard LLC converter. Mode 3 is not present in this converter as it works at resonance frequency.

1. Mode 1 corresponds to dead-time duration where no power is transferred to secondary. Primary current charges drain source capacitance of MOSFETs Q6 and Q7. The current also discharges that of MOSFETs Q5 and Q8 following which it conducts through antiparallel diodes of MOSFETs Q5 and Q8.
2. Mode 2 corresponds to the instant when MOSFETs Q5 and Q8 are turned ON at zero voltage since body diodes are already conducting. The primary current changes its direction to positive and power is transferred to secondary. Magnetizing current builds up slowly but L_m doesn't participate in resonance. Mode 2 ends at resonance operation i.e when primary current equals the magnetizing current. Also, power transfer to secondary stops at the end of mode 2.
3. Mode 3 starts when instantaneous primary current meets the magnetizing current. Secondary current is zero and primary current is same as magnetizing current. Magnetizing inductance and primary side resonance elements form a resonant tank till MOSFET Q5 turned OFF.

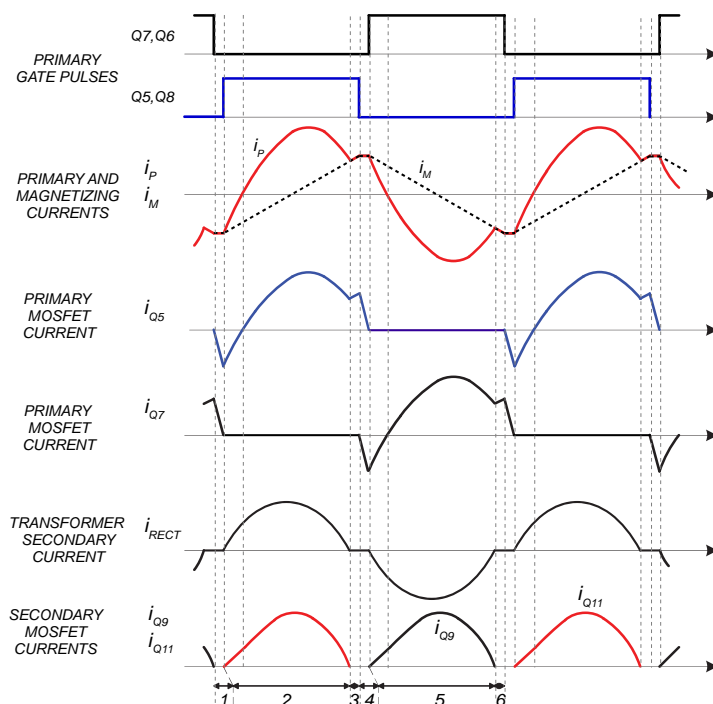


Figure 18. CLLC converter waveforms in charging mode

4. Mode 4 is again the dead-time duration same as mode 1 but the internal capacitors of MOSFETs Q5 and Q8 are charged and that of MOSFETs Q6 and Q7 are discharged.
5. Mode 5 is similar to the mode 2 where MOSFETs Q6 and Q7 turned ON at zero voltage and power is transferred to secondary diodes of MOSFETs Q9 and Q12.
6. Mode 6 corresponds to end of resonance in primary and power transfer to secondary. Also, it corresponds to beginning of resonance involving the magnetizing current as in mode 3.
7. The converter works higher than the resonance frequency during the start and gain is less than unity under that condition so that it can slowly charge the output capacitors.

DC-DC Converter Design:

Design of the resonant network can be an iterative process because the choice of components affects performance parameters like efficiency, regulation, operating frequency range, power loss and individual component stress. Following are some of the design considerations. Designing the converter means selecting resonance components and transformer magnetizing inductance apart from turns ratio and dead time. Based on some experimental results and optimizations, some basic resonant parameters are selected.

Transformer Turns Ratio:

Considering minimum DC link voltage of 390V and operation at resonant frequency (gain = 1) and minimum output voltage of 250V, the turns ratio with assumption of ideal switches will be:

$$n = \frac{390 \times 1}{250} = 1.56 (\text{ratio of 1.5 is selected})$$

Resonant frequency for both primary and secondary:

$$F_r = 200 \text{ kHz}$$

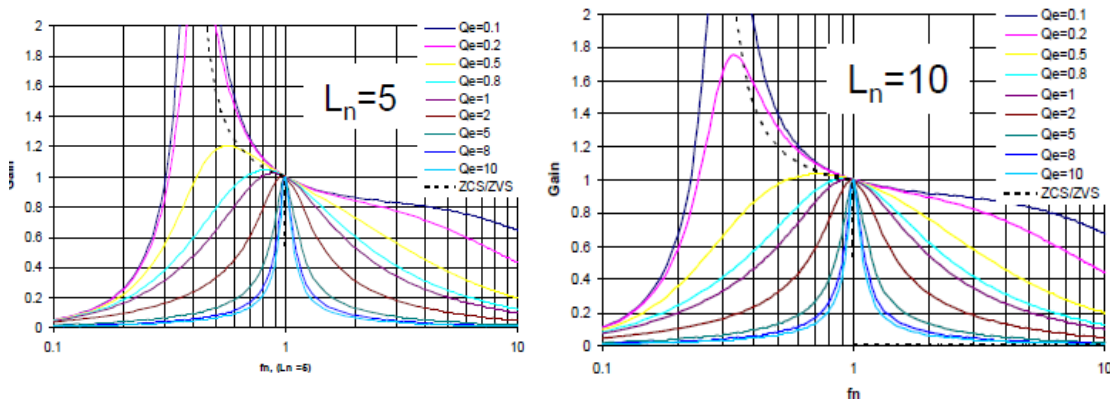


Figure 19.2 Gain VS frequency characteristics of LLC resonant converter

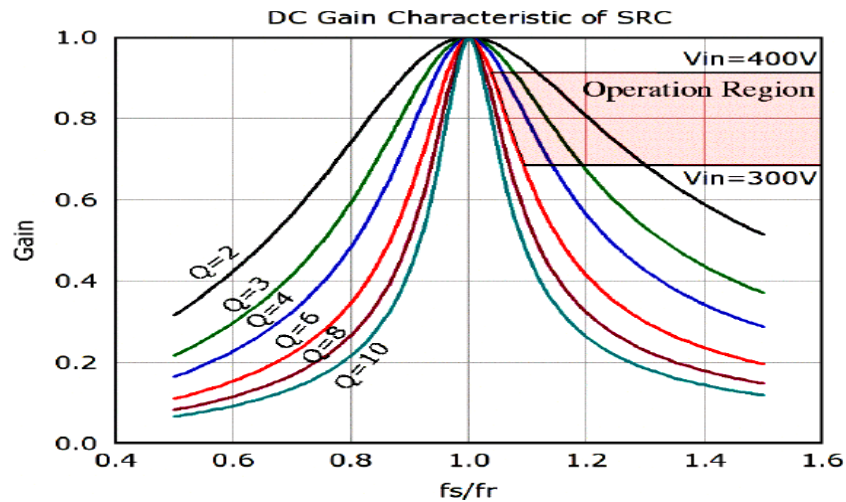


Figure 20. Gain Vs frequency characteristics of Series resonant converter

Ratio of magnetizing inductance to resonance inductance L_n : The converter voltage gain and operating frequency range depends on L_n . If L_n is small, the operating frequency range is small and vice-versa which is not required here. Value of L_n , thus can be independently selected of operating frequency. The question here is that if gain characteristic is no longer required, then what should be design criteria for L_n . For a very high value of L_n , the converter de-generates into a series resonance converter. Below figures show the characteristic of a LLC resonance converter and series resonance converter. The difference is that gain of series resonance converter drops sharply both above and below resonance frequency.

A value of $L_{n(100\mu H)} = \frac{L_m}{L_r} = 8$ has been selected here, but a ratio of 10 or even 12 should work equally well. Higher value of L_n shall require a smaller air gap in the transformer which is a desirable property to reduce flux fringing in the air gap. Higher the value of L_m also means smaller magnetizing current and less conduction losses in transformer.

Design of resonance inductor and capacitor values:

Let us define $L_{eq} = L_{rp} + L'_r$

& $C_{eq} = C_{rp} + C'_r$

$$Q_p = \frac{L_{eq}}{C_{eq}} \text{-----Value of Q as seen from the primary side}$$

$$Q_p = \sqrt{\frac{L_{eq}}{R_{LAC}}} \text{ where } Q_p \text{ is the value as seen from the primary side.}$$

A starting point for the design of resonance tank can be given now as:

$$\begin{aligned} Q_p &= .5 \\ L_{rp} &= L'_r \\ C_{rp} &= C'_r \\ L_m &= L_n * L_{rp} \\ F_r &= 200 \text{ kHz} \end{aligned}$$

Following the above criteria, table below shows the components values obtained:

| | L_{rp} | L_{rs} | C_{rp} | C_{rp} | L_m |
|--------------------------|----------|----------|-----------|--------------|-------|
| values | 11uh | 4.88uh | 56nf | 126nf | 88uh |
| Full load Voltage stress | | | 280V(RMS) | 185.12V(RMS) | |

Table 6. Specifications of DC-DC Stage

Where the value of voltage stress across the resonance capacitors have been obtained by the below equation:

$$\text{Peak input current on primary side} = I_{pri} = \frac{6600 * \pi}{390 * .95 * 2} = 27.98A$$

$$\text{Peak input current on secondary side} = I_{sec} = \frac{6600 * \pi}{250 * 2} = 41.46A$$

Here an efficiency figure of 95% has been assumed for the input current and 100% efficiency has been considered for the secondary side current. 6600W is the rated power and 390VDC and 250VDC are the minimum input and output voltages of CLLC converter.

Peak voltage stress on resonance capacitors on primary and secondary side are given by:

$$\text{Peak voltage stress on primary resonance capacitor} = V_{pri} = \frac{I_{pri}}{2 * \pi * F_r * C_{rp}} = 397V$$

$$\text{Peak voltage stress on secondary resonance capacitor} = V_{sec} = \frac{I_{sec}}{2 * \pi * F_r * C_{rs}} = 261.8V$$

Below table shows the actual values which have been used for this prototype:

| | L_{rp} | L_{rs} | C_{rp} | C_{rp} | L_m |
|--------------------------|----------|----------|-----------|-----------|-------|
| values | 12uh | 8uh | 56nf | 84nf | 100uh |
| Full load Voltage stress | | | 280V(RMS) | 277V(RMS) | |

Table 7. Actual Values of CLLC resonant components used for prototype

Selection of Capacitors:

Film capacitors are used for primary and secondary resonance capacitors. Voltage and current rating of these film capacitors must be verified. Voltage rating required must satisfy as given in the table 7 and current rating is equal to the RMS current on primary and secondary sides respectively. Voltage rating of film capacitors reduces significantly as shown in the Figure 21.

As shown in Figure 21, 6.8nf cap can be used up to 250V and 2.2nf can be used up to 375V. Taking into the consideration of some safety margin, we have decided to use 4.7nf capacitor which should be good for both primary side and secondary side.

Power dissipation in resonance capacitors: at 400V input and 250V output:

Measured value of ESR on LCR meter=35mohm

$$\text{Power dissipation in each primary resonance capacitor} = I_{pri}^2 * R = 19.8^2 * \frac{0.035}{12} = 1.14W$$

$$\text{Power dissipation in each secondary resonance capacitor} = I_{sec}^2 * R = 27.8^2 * \frac{0.035}{18} = 1.67W$$

$$\text{Power dissipation in each primary resonance capacitor} = .095W$$

$$\text{Power dissipation in each secondary resonance capacitor} = .083W$$

1250 V DC/450 V AC

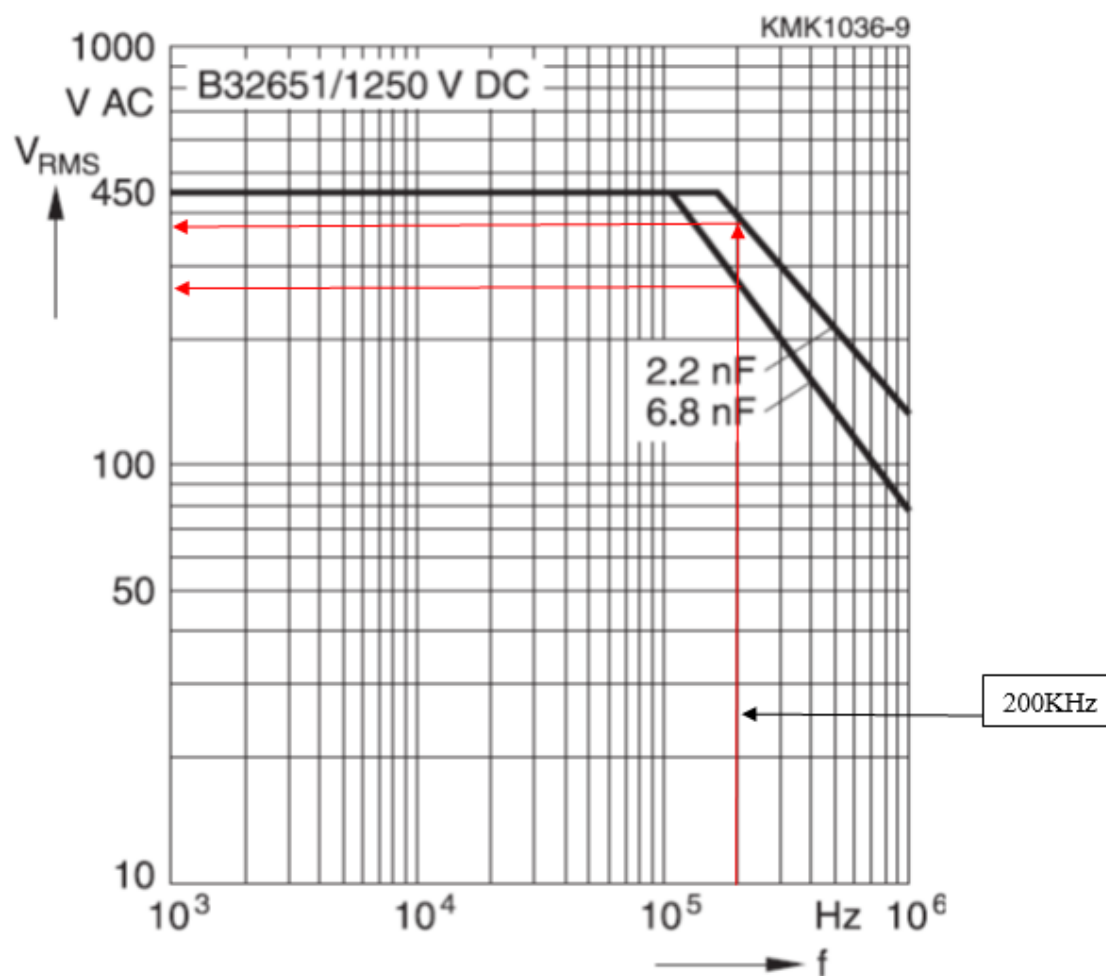


Figure 21.3 Frequency Vs AC Voltage rating of resonant capacitor

Following table indicates the details of resonance inductor:

| | value | Core | turns | Rdc | Res loss | Cor loss |
|----------|-------|------------|-------|---------|----------|----------|
| L_{rp} | 12uh | EE42/21/15 | 18 | 9.8mohm | | |
| L_{rs} | 8uh | EE42/21/15 | 12 | 4.6mohm | | |

Table 8. CLLC Resonant inductor's details

Design flow chart of CLLC Bi-Directional resonance converter:

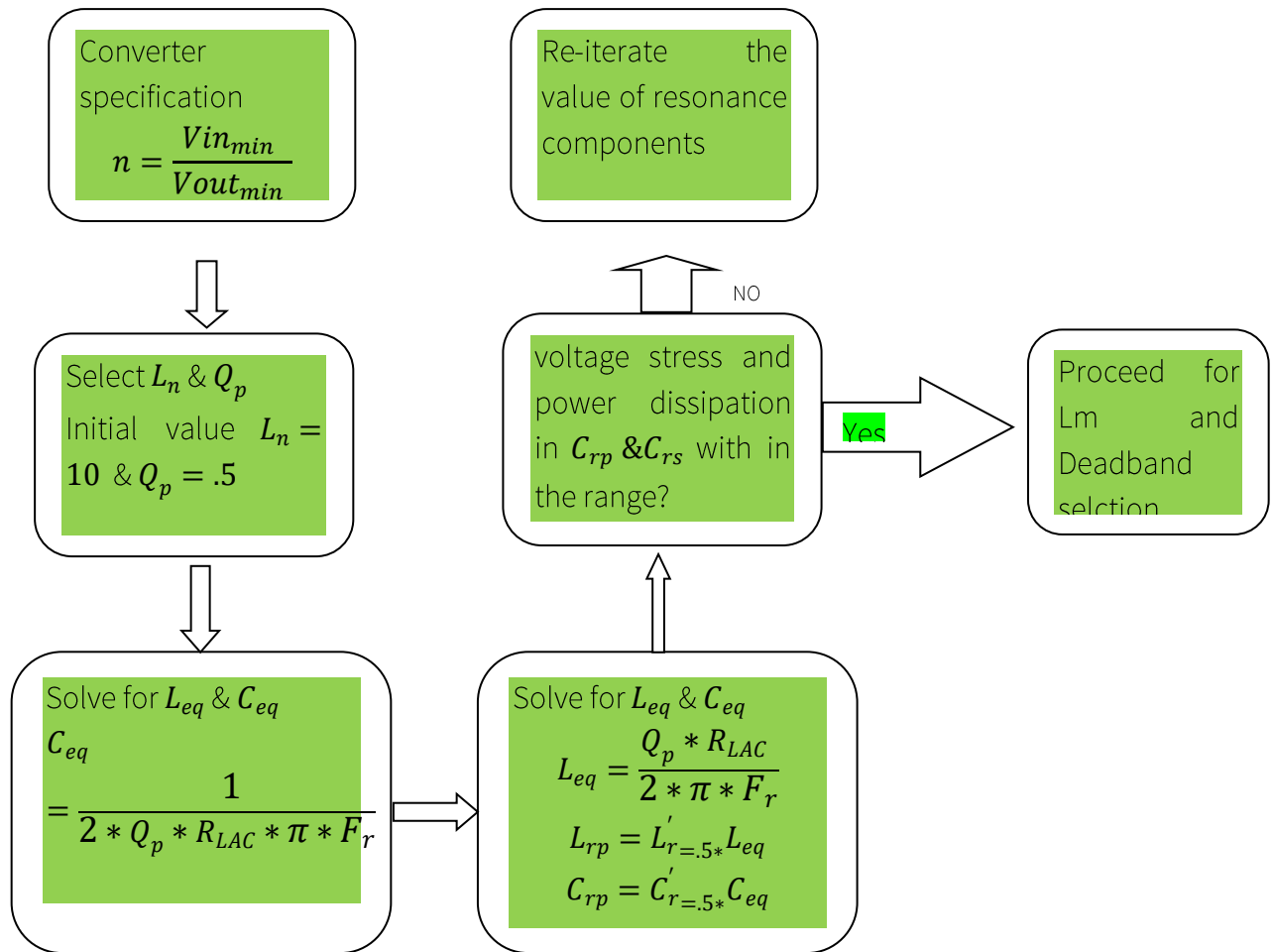


Figure 224. Design flow chart of CLLC Bi-Directional Resonance Converter

A check on the value of magnetizing inductance:

A fixed frequency DC/DC converter provides some freedom in choosing magnetizing inductance L_m as compared to a variable frequency inverter but the value has still to be designed to ensure that ZVS of the primary switch happens during the dead time. Following methodology can be adopted to check ZVS of primary switches.

$$.5 * (L_r * I_m^2 + L_m * I_m^2) \geq .5 * 4 * C_{oss} * V_{dc}^2$$

As $L_m \gg L_r$ this condition can be reduced to: (1)

$$.5 * (L_m * I_m^2) \geq .5 * 4 * C_{oss} * V_{dc}^2$$

where C_{oss} is the energy related output capacitance of the MOSFET:

I_m (magnetizing current) can be given as:

$$I_m = \frac{V_{dc} * T}{L_m * 4}$$

Putting value of I_m in equation 1:

$$L_m = \frac{T^2}{(64 * C_{oss})}$$

Putting the actual value for this design $T=5\mu\text{sec}$ and $C_{oss}=80\text{pf}$, the value of $L_m=4882\mu\text{H}$.

This is the maximum value of magnetizing inductance above which energy in magnetizing inductance is less than the C_{oss} energy. In fact, the value of magnetizing energy must be more than 10 times the capacitive energy so that magnetizing current remains constant during the dead time which may put a limit of $L_m=488\mu\text{H}$ for this application.

We have another constraint here based on the dead time. ZVS of the primary switch must happen during the dead time provided. If the magnetizing current I_m remains constant during dead time (T_d) (correct assumption if energy in L_m is much larger than capacitive energy), it can be assumed that I_m charges and discharges C_{oss} linearly.

$$I_m = \frac{4 * C_{oss} * V_{dc}}{T_d}$$

By putting the value of I_m in L_m equation:

$$L_m = \frac{(T_d * T)}{(16 * C_{oss})}$$

Again, putting a dead time of 200nsec and previous value of other parameters. We get $L_m = 781\mu\text{H}$ (this is another high limit which affects the dead time). Again, L_m value must be lower than this value so that ZVS is obtained within the dead time. Preferably, more than 100% margin so that other parasitic capacitances and variation in C_{oss} of the MOSFETs are taken into consideration.

We have chosen a value of $100\mu\text{H}$ for this design but a value of more than this; preferably $200\mu\text{H}$ could be more appropriate.

The frequency Vs gain characteristics at 10% of load, 50% load and 100% load are given in figure (23) & (24). These gain curves have been obtained by simulation and using values which have been used in actual prototype. There is not much difference between $100\mu\text{H}$ and $200\mu\text{H}$ curves except at very light load. This converter is supposed to work at resonance frequency with unity gain so it makes sense to have a higher magnetizing inductance and consequently lower magnetizing current. That increases the efficiency due to lower overall current in transformer.

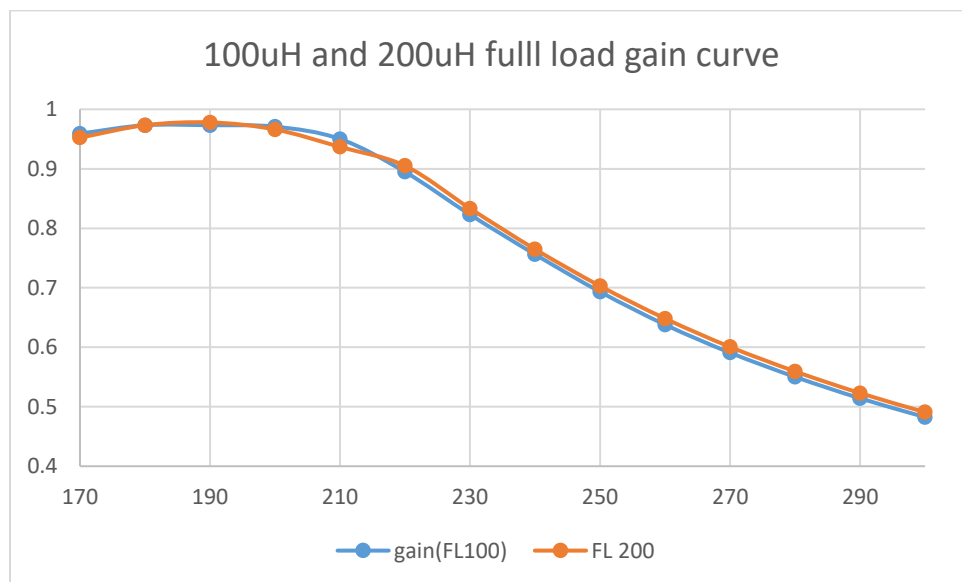


Figure 235. Gain VS Frequency of CLLC for $100\mu\text{H}$ and $200\mu\text{H}$ L_m @ full load

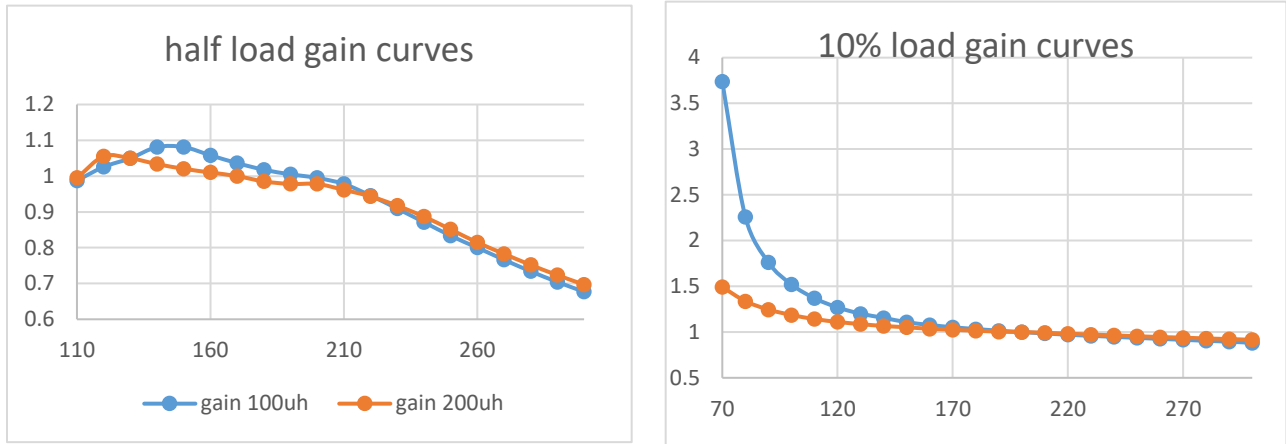
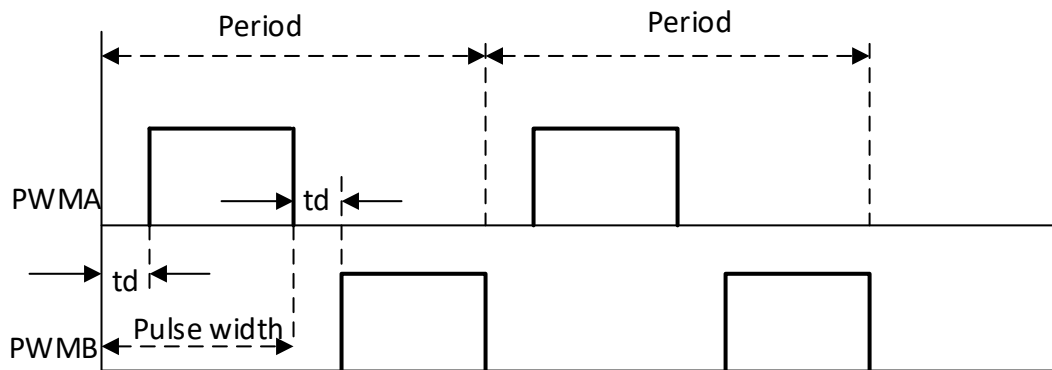


Figure 246. Gain VS Frequency of CLLC for 100uH and 200uH Lm @ Half load and 10% load

Selection of dead time for primary CLLC MOSFETs:

Complementary (top & bottom) MOSFETs of CLLC converter are gated after a dead time of T_d (as shown in Figure 25).



t_d =Dead band delay

Figure 25. CLLC Gate waveform showing deadtime

Now, design of this dead time is important for the converter operation. Apart from ensuring that the complementary MOSFETs do not get shorted, another very important function of dead time is to provide ZVS of CLLC MOSFETs. Too little or too high a dead time affects the converter operation and efficiency as shown in Figure 26.

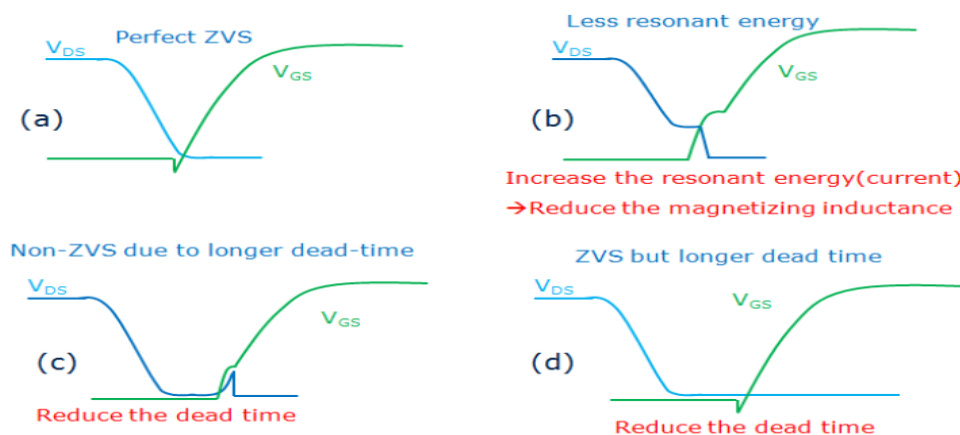


Figure 26. CLLC deadtime and ZVS relation

Equation for dead time for full bridge CLLC converter is given by:

$$T_d = 4 * C_{oss}(cir) * \frac{V_{dc}}{I_{mag}}$$

where $coss(cir)$ is the MOSFET output capacitance (circuit related).

If we assume $coss=80\text{pf}$; for 1000V, 65mohm part:

$T_d=4*80\text{e-}12*400/5=25.6\text{nsec}$ for 400v DC bus

$T_d=4*80\text{e-}12*680/8.5=25\text{nsec}$ for 680V DC bus

Note: Only this computation is based on a circuit related C_{oss} of 80pf which probably is not correct.

Following dead times can be tabulated for magnetizing inductances of 100uH and 200uH:

| | 100uH | 200uH |
|-------------|-----------|-----------|
| 400V DC bus | 25.6 nsec | 51.2 nsec |
| 680V DC bus | 25 nsec | 50 nsec |

Table 9. Dead time required for 100uH and 200uH Lm

It appears that T_d is independent of DC bus voltage magnitude because I_{mag} also changes with the DC bus voltage. Dead time given in the present design is 200nsec so either we land with condition (c) or condition (d). Condition (d) only results in some loss of duty cycle but condition (c) results in non-ZVS condition of the converter. If resonance frequency of the converter is high, condition (c) is more likely due to short resonance current period.

Computation to avoid condition (c):

Condition (c) must be avoided due to 4 reasons: 1.) extra reverse recovery losses in MOSFET body diode 2.) loss of duty cycle 3.) disruption in normal resonance cycle & 4.) non-ZVS condition during switch ON. Let us define the maximum value of dead time to avoid (c)

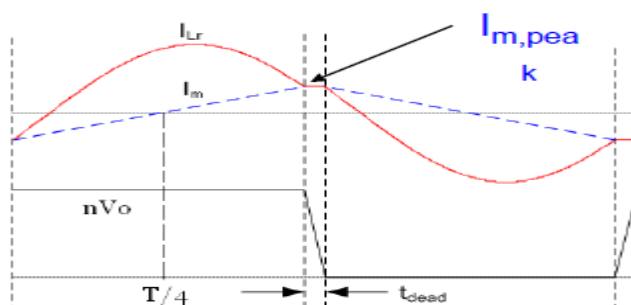


Figure 26. CLLC deadtime and ZVS condition

If the dead time is extended beyond the value shown in Figure 26, I_{mag} decreases linearly and normal resonance cycle occurs through the body diode of the MOSFETs. If pulses are switched ON before the primary current has gone to zero then the normal resonance continues through the MOSFET, otherwise the total primary current comes to zero, buildup of magnetizing current

stops at zero and body diode starts recovering. This buildup the voltage in the MOSFET and leading to non-ZVS condition.

Equation for current beyond when voltage across the MOSFET has gone to zero can be written as:

$$I_{mag} * (1 - t / (.25 * T)) = I_{peak} * \sin(wt)$$

Now I_{peak} for a 6.6KW converter at 400V DC bus is given by 26A and for 680VDC bus is given by 15.2A.

The primary current reaches zero when magnetizing current= $I_{peak}(\sin(wt))$

The above equation thus can be solved to get a correct value of time which can be allowed beyond computed dead time given in Table 9. Since the equation is non-linear, it can be solved numerically and values for 400VDC bus and 680VDC bus are given in the Table 10.

| 400V DC bus condition (time) | I_{mag} (Amp) | $I_{peak} * \sin(wt)$ (Amp) |
|------------------------------|-----------------|-----------------------------|
| 50nsec | 4.8 | 1.6 |
| 100 nsec | 4.6 | 3.25 |
| 150 nsec | 4.4 | 4.87 |
| 200 nsec | 4.2 | 6.46 |

Table 10. Computed Dead time for 400V DC bus condition

It is clear from the Table 10 that at around 150 nsec, resonance current is equal to magnetizing current and extending the dead time above ((150 nsec+25 nsec) =200nsec)), it would lead to non-ZVS condition. Similar way the Table 11 can be given for 680V condition.

| 680V DC bus(time) | Imag | I _{peak} *Sin(wt) |
|-------------------|------|----------------------------|
| 50 nsec | 8.16 | .95 |
| 100 nsec | 8.14 | 1.9 |
| 150 nsec | 7.48 | 1.64 |
| 200 nsec | 7.14 | 3.78 |
| 300 nsec | 6.46 | 5.59 |
| 350 nsec | 6.12 | 6.47 |

Table 11. Computed Dead time for 680V DC bus condition

For 680V operation, this condition arrives at around 300nsec which can be tolerated up to (300+25)= 325nsec (maximum delay).



Figure 27. Comparison of ZVS for 400V (Left) and 680V (Right) Operation

The oscilloscope waveforms (as shown in Figure 27) show the validity of the concept. On the left side of Figure 27, from 400v operation and 300 nsec dead time, It clearly shows the effect of NON-ZVS condition (green waveform dip), while from 680V operation (Right side of Figure 27), the same dead time does not show non-ZVS condition. This dip vanished when the dead time was brought down to 200nsec. The also equates that at light load, this phenomenon does not occur because Imag takes around T/4 time to go to zero.

Selection of dead time between primary CLLC MOSFETs and secondary CLLC MOSFETs:

Another important criterion is to select the dead time between the turn ON of the primary CLLC MOSFETs and secondary synchronous MOSFETs. ZVS of synchronous MOSFETs happens due to the resonance load current.

Again, the dead time required shall be defined by the equation:

$$T_{dead} = \frac{4 * C_{oss} * v_{out}}{I_m * \sin(\omega t)}$$

where I_m is the load current amplitude in secondary.

Integrating the above equation, we get

$$T_{dead} = \frac{\cos^{-1}(1 - C_{oss} * V_{out})}{I_m}$$

This equation can be solved for the dead time which is load current dependent. It is clear that the lower load requires higher dead time and vice versa. Failure to observe this condition may result in non ZVS operation of the synchronous MOSFETs.

DC-DC Transformer Design:

Input voltage = 480V rated at 320V battery output

Output voltage = 320V

Maximum output power = 6600W

Maximum output current = 22A

DC DC normal efficiency = 98%

Turns ratio = $n = \frac{V_{PFC_{nom}}}{V_{O_{nom}} + 0.5} = 1.5$

$$I_{O_{nom}} = \frac{P_o}{V_{O_{nom}}} = 20.625A$$

Transformer Window Coefficient $K_{W_t} = 0.35$

Set $B_{max_t} = 0.12T$ single quadrant

Primary current density $J_{max_{tp}} = 5A/mm^2$

Frequency of DC DC = $f_{req_{dcdc}} = 200kHz$

Minimum required AeAw of the transformer = $\frac{L_m * I_{pknom} * I_{rmsnom}}{B_{max} * K_w * J_{max_{tp}}} = 1.901 * 10^{-7} m^4$

For PQ50 50

Ae=328mm²

Number of secondary turns = $N_{ts} = \frac{V_{onom} + 0.4}{4 * B_{max} * A_{epq5050} * f_{req_{dcdc}}} = 10.213$

Max number of secondary turns = $N_{ts_{max}} = \frac{V_{omax} + 0.4}{4 * B_{max} * A_{epq5050} * f_{req_{dcdc}}} = 14.342$

Actual secondary turns = 12

Actual Primary turns = 1.5 * 12 = 18

Air gap required = $l_{g_{tf}} = \frac{\mu_0 * N^2 * A_{epq5050}}{L_m} = 1.423 * 10^{-3} m$

Based on the skin depth, AWG38 of litz wire 350 numbers in parallel are used in primary and

Total DC resistance of the transformer primary = 13.7mohm

Total DC resistance of the transformer secondary = 5.46mohm

4.1.3 Control Structure of the Converter

There are 2 completely separate converters running in cascade: a) Totem-pole PFC converter and b) fixed frequency CLLC converter. Both are bi-directional and both run independently. PFC converter has a 2 loop structure (as shown in Figure 33) where there is an outer voltage loop to control the DC link voltage which generates the reference for inner current loop which further maintains a sinusoidal current in phase with the input grid voltage. CLLC converter always runs at fixed frequency (resonance) and does not have any kind of closed loop control.

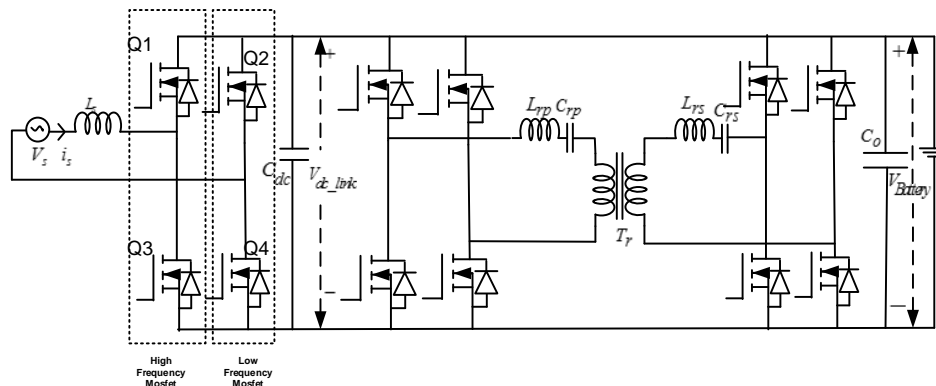


Figure 28.7 System schematic diagram

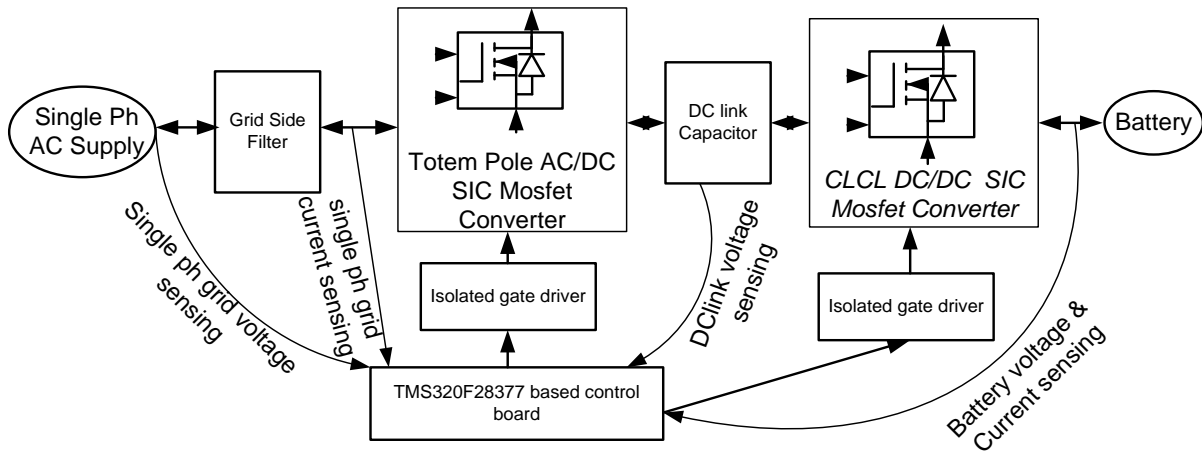


Figure 29. Signal interconnection diagram

Figure 29 shows the control block diagram of the converter as implemented. Control blocks have been implemented on Texas Instruments (P/N: TMS320F28377) Delfino floating point processor. Please refer to the schematic of the DSP board for detailed hardware circuit description. Coding has been done in CCS platform.

Referring to the control block Figure 33, V_{dc_ref} is set based on output voltage and v_{dc_fb} is the DC link voltage. PI voltage controller is implemented based on PI compensator whose frequency band width is set to a low value. Current reference thus generated is added with output current which acts as feed forward for fast dynamic response. Resulting signal is multiplied with sinusoidal signal obtained from PLL to set the current reference for the current loop. This reference signal is in phase with input grid voltage and tracks it at every point in time.

Selection of PLL for the converter:

PLL is required to track the phase and frequency of the signal in a grid connected system. A robust PLL should be able to track the grid voltage and frequency despite considerable noise in the system and should be fast enough to detect a phase or frequency change. Commonly adopted PLL configurations for single phase systems are inverse park PLL, second order generalized integrator (SOGI) PLL and enhanced PLL (EPLL).

It has been widely reported in the literature that EPLL is least sensitive to disturbances like DC bias, harmonics and phase jump. So, EPLL was adopted for this converter. Figure 28 shows the block diagram of EPLL.

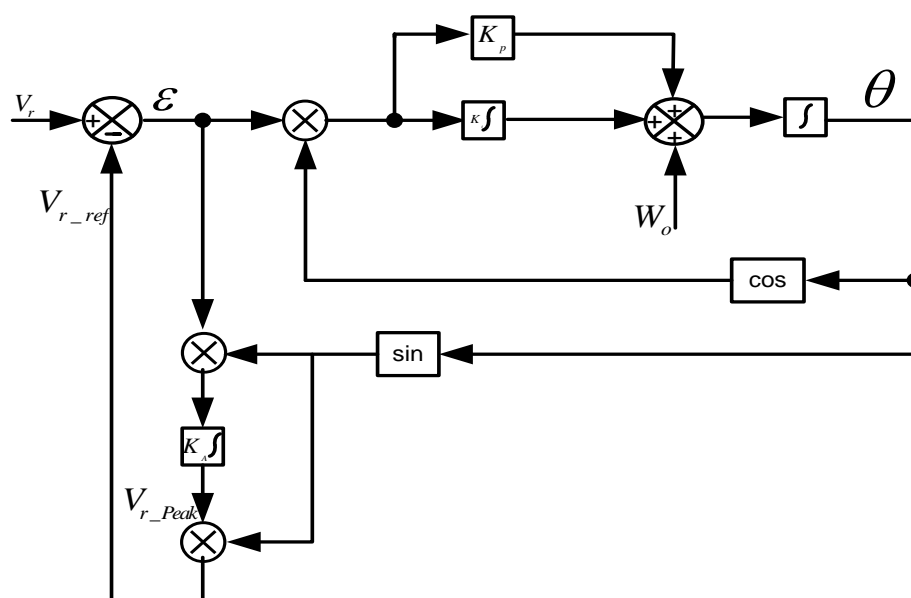


Figure 30. EPLL block diagram

There are 2 types of controllers which act on the current error obtained after the subtraction block. First is typically used as a PI compensator and second is a string of resonance controllers. It is well known that PI compensators are good for DC signals. The error signal here is sinusoidal and the integral part in PI compensator leads to a phase difference between the error signal and its response because unlike a DC signal it cannot settle to a steady state value. Figure 31 shows the response of various compensators to the sinusoidal signal. It can be seen that the integral response is delayed by 90 deg. and the proportional response exactly mimics the input signal. PI response thus would be an addition of the response of P and I signals.

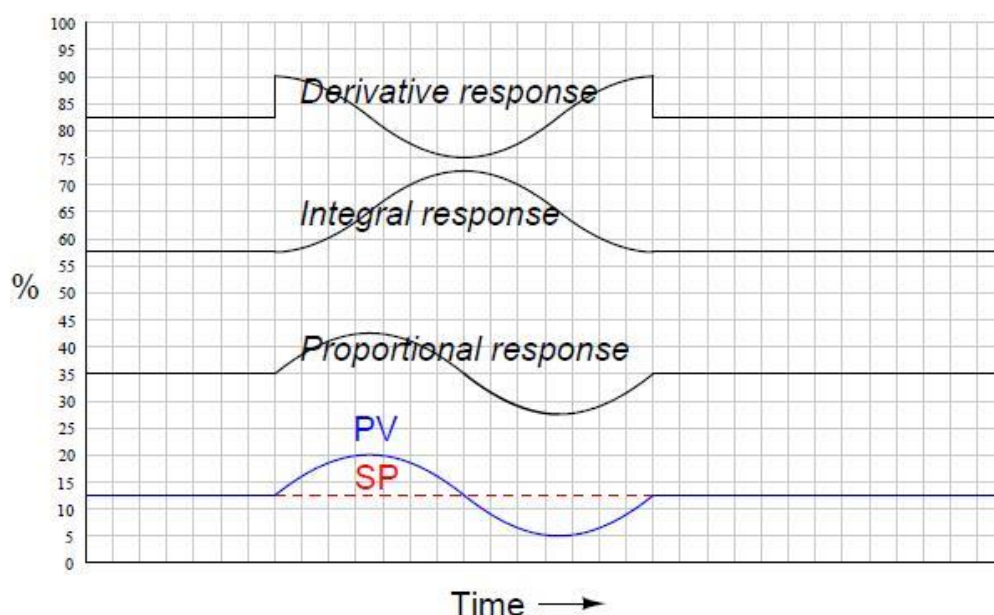


Figure 31. Response of various compensators to the sinusoidal signal

Delayed response of the controller is of course undesirable and would lead to phase error in tracking as well as overshoot and undershoot under transient conditions. One way to solve this problem is to have a larger P part and smaller I part but P part larger than a certain value leads to oscillations. If we are using DSP, in that case P & I can be tuned for different values of load and best values of $P * I$ can be tabulated in the processor. The problem of phase lag can be more severe if the error signal consists of signals which are the harmonics of fundamental and very difficult to be compensated without considerable phase lag.

A better approach could be to use resonance controller for time varying signals. If it is assumed that the error signal consists of a DC part and various harmonics of sinusoidal signals, then DC part can be compensated with normal PI compensator and AC portion can be compensated with resonance controllers. Since, resonance compensators are tuned to a particular frequency, not all harmonics can be compensated and those which are dominant should be compensated. In this application, it can be safely assumed that the error signal does not have a DC component and it consists of fundamental of line frequency and its harmonics. In that case, the fundamental can be compensated with PI controllers and harmonics can be compensated with resonance controllers. It is possible to compensate fundamental with the resonance controllers as well.

| controller | Transfer function |
|--------------|---|
| PI | $K_p + \frac{K_i}{s}$ |
| Ideal PR | $K_p + K_i \left(\frac{s}{s^2 + \omega_0^2} \right)$ |
| Practical PR | $K_p + K_i \left(\frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \right)$ |

Table 12. Controllers and their transfer functions

Response of the PR controller is shown in the Figure 32.

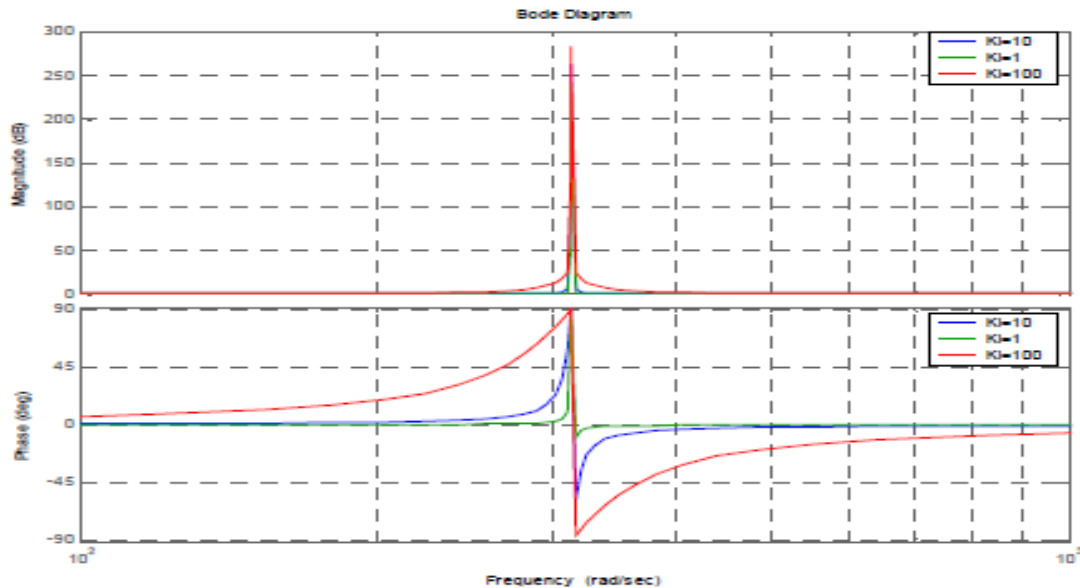


Figure 32. Response of resonance controller tuned to a particular frequency

Figure 32 shows that the response of resonance controller is tuned to a particular frequency, it has ideally infinite gain for the selected frequency and no gain for the other frequency components. In this application, PI compensator has been used for the fundamental frequency and resonance controllers have been used for 3,5,7 and 11 th harmonics.

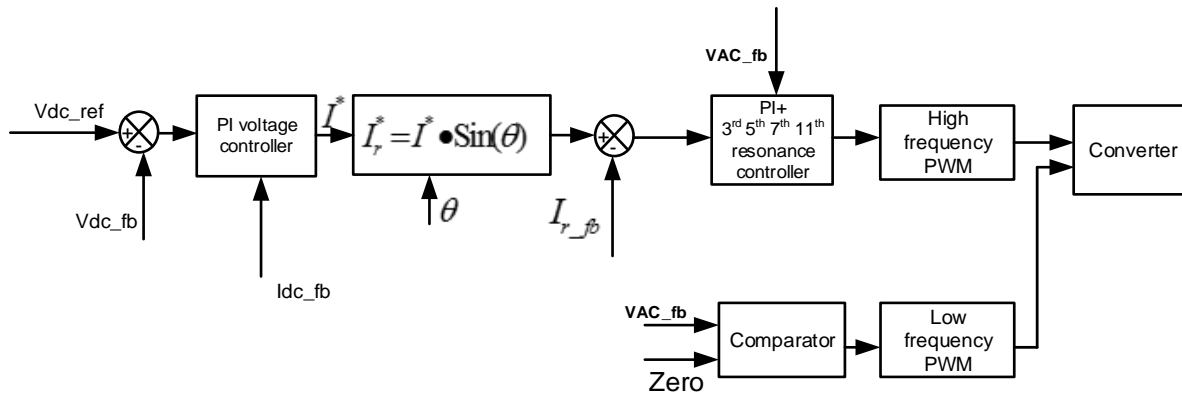


Figure 33. System Control Block Diagram

4.1.4 Gate Drive Circuitry

The gate drive circuitry is based on isolated gate driver ICs with up to 1200V isolation on the high voltage side and 3.75kV isolation on the battery side. A dual rail supply for preventing unintentional turn ON of MOSFETs. The gate drive power required with a gate drive voltage swing of 15V and -2.5V is:

$$P_{gate(ac-dc)} = V_g Q_g F_s = (15 + 2.5) \times 35n \times 67k = 0.04W$$

$$P_{gate(dc-dc)} = V_g Q_g F_s = (15 + 2.5) \times 35n \times 200k = 0.122W$$

The isolated dual polarity gate driver supplies for each driver IC is generated from an isolated DC-DC converter module (P/N: QA15115) powered up by external 15V source as in Figure 34. The power supply module generates dual supply of +15V and -2.5V with each output capable of handling 100mA current. The module also provides isolation of up to 3.5kV.

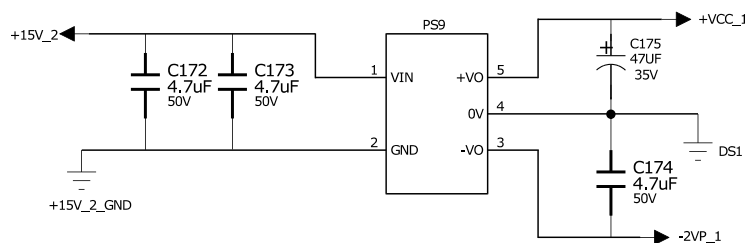


Figure 34. Gate driver supply using QA15115R2

Note: while choosing an isolated driver, be careful about the Input/output parasitic capacitance.

Gate Drive Circuitry for High Voltage Side MOSFETs:

The high voltage side MOSFETs are driven using Infineon gate driver (P/N: 1EDI30I12MHXUMA1) (as shown in Figure 35). The driver features 3A peak source and sink current capability, up to 1200V isolation and active miller clamp for gate which along with the negative supply provides an additional protection against parasitic turn ON of the MOSFET. The input is driven from 3V to 15V range signals and support direct CMOS level signals.

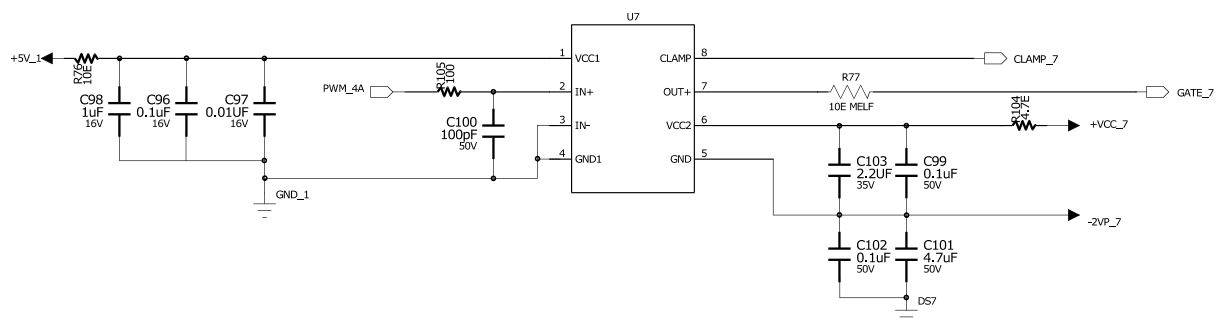


Figure 35. Gate drive circuitry with IEDI30I12MHXUMA1

The non-inverting PWM input to the driver comes from the controller through a 5V output level buffer. A small filter network (R105 and C100) is placed close to input pins. The buffered input and 5V bias supply is routed from the control card. RC filtering of the control and driver side supply provides another level of supply noise immunity. The driver output is connected to the gate pin through the gate resistance and the clamp pin is directly connected to the gate pin close to the MOSFET.

Other functional features with the gate driver IC are:

1. Operating bias voltage of up to 17V on input side and 18V on output side. Under-voltage protection at 2.85V and 12V on input and output sides respectively below which the output is held low.
2. Low internal voltage drop in driver ensuring minimal dissipation in driver
3. Clamping of the gate voltage to supply voltage when the gate voltage rises in the event of short circuit because of feedback through Miller capacitance

- Active Miller clamp protection (when the MOSFET even in OFF state) can turn ON in a half bridge configuration. The dv/dt of the MOSFET while turning ON causes a current to take path through the gate pin. The clamp pin sinks this current across a low impedance path by monitoring the gate voltage

Note: Be careful about the propagation delay through the driver.

Gate Drive Circuitry for Battery Side MOSFETs:

The battery side MOSFETs are driven from an isolated gate driver (P/N: SI8261BCC-C-IS) (as shown in Figure36). The driver is capable of supporting gate current of up to 4A with input to output isolation of about 3.75kV. The output of the driver follows the input current through the LED. The current through the input LED of driver should be greater than 6mA for output to rise. To support this current, a non-inverting buffer IC (P/N: MCP1402) is used.

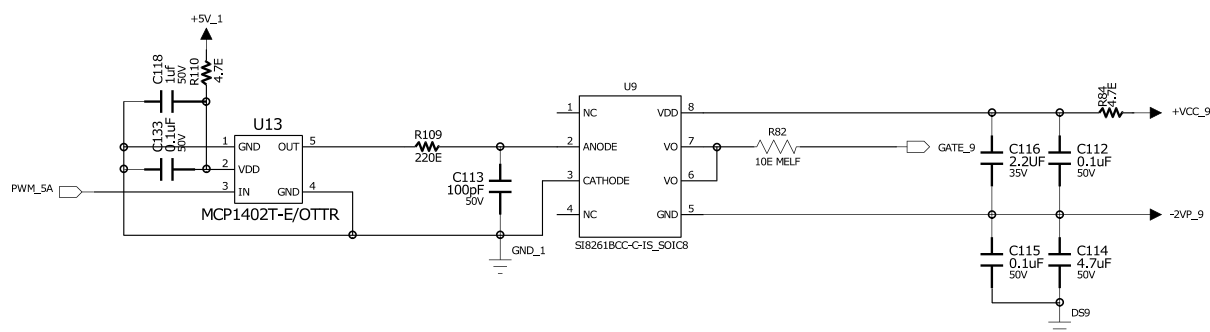


Figure 36. Gate drive circuit using SI8261BCC-C-IS

The input of the buffer is TTL and CMOS logic level compatible and is driven by a level shift IC in control card. The output is non-inverting and has peak voltage magnitude of 5V. The input current to the driver IC is limited by using a current limiting resistor such that:

$$I_F = \frac{5 - V_F}{R_F} > (I_{Fon} = 6mA)$$

The driver input current is limited to 10mA. With the maximum LED forward drop voltage of 2.8V, the current limiting resistor selected is 220Ω.

On the driver output side, the isolated supply is generated through isolated DC-DC converter modules (as shown in Figure 34). The driver IC has a UVLO threshold of 7.9V and 0.5V hysteresis below which the output is pulled low irrespective of input current. A similar feature is implemented for input LED current also (as shown in Figure 37).

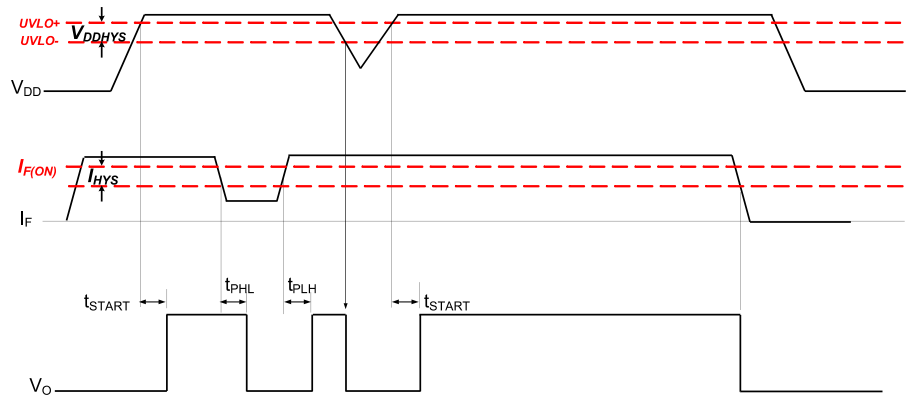


Figure 37. Input and output supply protections for Si8261BCC

The internal resistances of the driver will dissipate some power depending on the current drawn by the gate, the power dissipated in input diode and the IC internal power consumption is:

$$P_{driver} = (V_{DD}I_{DD}) + (V_F I_{Favg}) + \left(\frac{1}{2} Q_G V_G F_{SW} \left(\frac{R_{OH}}{R_{OH} + R_G} + \frac{R_{OL}}{R_{OL} + R_G} \right) \right)$$

The driver current requirement I_{DD} , the ON and OFF resistances R_{OH} and R_{OL} are obtained from driver datasheet. The average input current depends on peak input current and duty cycle of gate pulse. A part of the gate drive power is dissipated in resistances of transistors of driver output stage R_{OH} and R_{OL} . The maximum power dissipated in driver is:

$$P_{driver} = (17.5 \times 2.5m) + (2.8 \times 10m \times 0.5) + \left(\frac{1}{2} 35n \times 17.5 \times 200k \left(\frac{5.1}{5.1 + 10} + \frac{2}{2 + 10} \right) \right) =$$

$$P_{driver} = 0.088W$$

The maximum possible power dissipation in the driver is 1W to prevent the junction temperature reaching the maximum allowed limit 140°C, when operating at ambient temperature of 25°C. With the calculated power dissipation, the maximum temperature in the driver is 35°C.

Gate Resistor Calculation and Selection:

The gate resistors are calculated to ensure that the peak gate currents during turn ON and OFF are within the maximum capacity of the driver and the minimum internal resistance of MOSFET gate and the driver IC. Furthermore, the resistance can be increased or decreased. A 10Ω gate resistance is used for all the MOSFETs. A 1Ω resistor close to the MOSFET gate and source pins together limits the peak gate current to 1.46A when the gate voltage makes a transition from -2.5V to 15V during turn ON or vice-versa. For the AC-DC stage where two MOSFETs are paralleled, a single gate resistor from driver followed by two separate resistors close to each MOSFET gate are used.

The pulsed current will stay for a small duration, till MOSFET rise/fall time (of few nsec) and the resistor has to withstand repetitive pulsed power of:

$$P_{pulsed-gate} = \left(\frac{15 + 2.5}{10} \right)^2 \times 10 = 25.52W$$

The continuous pulsed current handling capability for resistors of standard package with respect to pulse width is shown in Figure 38. The package that can safely handle the pulsed power is 1206.

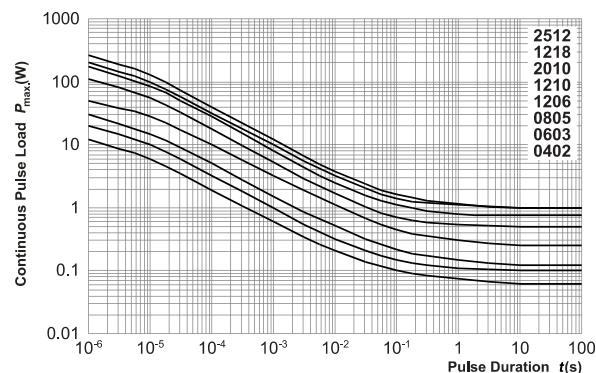


Figure 38. Pulsed power ratings for thick film chip resistors

4.1.5 Design and Layout Considerations for High Frequency Switching

SiC MOSFETs and diodes enable the switching frequency to go higher, 100kHz or more, without significant loss in efficiency as compared to the Si devices. The indirect benefits are reduction in filter size, cooling requirements and overall system cost. However, with high switching frequency and at high power levels, special attention to EMI minimization is required.

Kelvin Connection for Gate:

With a 3 pin MOSFET connection with a common source pin, the rate of decay of drain current during turn OFF causes a voltage drop across the parasitic inductance of source pin and trace. The induced voltage in opposition with the gate voltage causes a reduction in gate current and slows down the switching transition period. The MOSFET cannot reach its full switching transition capability and causes increase in the switching energies. Also, when devices are paralleled, the difference in stray inductances can cause imbalance in dynamic current sharing.

Cree's (C3MTM) 1000V, 65mΩ, C3M0065100K MOSFET come in a 4pin package with a separate pin for gate driver source connections as shown in Figure 39.

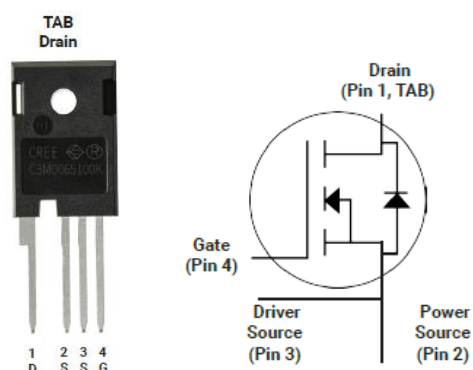


Figure 39. Cree's C3M0065100K in a TO-247-4 Package

The Kelvin source pin of TO-247-4 package along with the isolation in gate driver circuitry, provides benefit of very low inductance in driver source pin. The negative feedback effect due to

the inductance minimization, enabling faster switching and lower switching losses. The switching loss data for Cree's 3 pin (C3M0065090D) and 4 pin (C3M0065100K) package MOSFETs of same rating is shown in **Error! Reference source not found.**⁴⁰. There is a significant reduction in switching loss at higher currents.

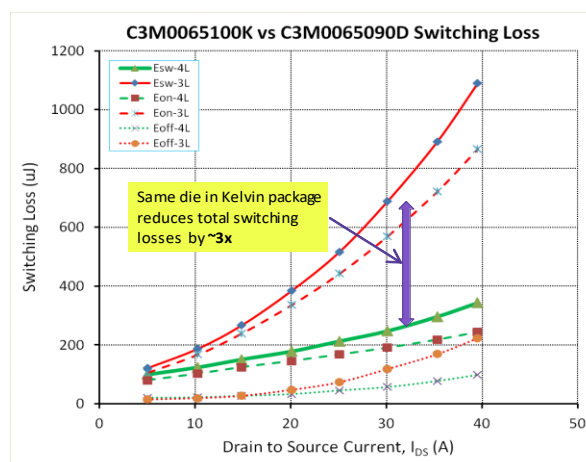


Figure 40. Switching energies of Cree's SiC MOSFETs in a TO-247-3 and TO-247-4 Packages

Layout considerations on the gate side:

Since the devices are in parallel position to achieve higher efficiency, the gate connections are designed to be symmetrical to aid in dynamic current sharing. The static current sharing is inherently achieved by the positive temperature coefficient characteristics of the ON state resistance and equal gate voltage to both MOSFETs. It is also important to reduce the switching loop in gate circuitry to minimize ringing in gate voltages, considering the low threshold voltage of the MOSFETs.

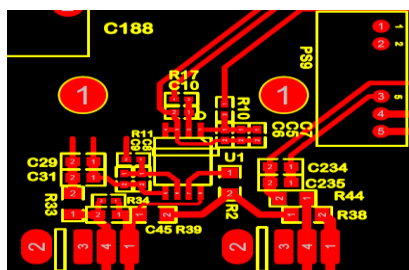


Figure 41. Gate connections to paralleled SiC MOSFETs

A section of gate side layout for Q1 and Q2 is shown in Figure 41. The gate driver is placed as close as possible to the MOSFETs. The gate driver and signals associated with the gate are placed on the top layer of PCB with the power traces running in the subsequent layers. The paralleled devices have a common gate resistor R2 following which the trace lengths to gates are equal for both. The decoupling capacitors on the -2.5V are placed close to the resistor from source pin to minimize loop inductance and provide tight coupling between source and -2.5V node.

The parasitic gate drain capacitance in the board is kept to a minimum so that it is below the MOSFET internal gate drain (miller) capacitance. At higher dv/dt situations, coupling of voltage rise in drain can affect the gate traces and cause spurious gate voltage transitions. The decrease in parasitic gate drain capacitance is also achieved by keeping sufficient distance between gate and drain tracks or by keeping them in different layers and avoiding any overlap between the two tracks. The effect can also be minimized by using higher gate resistance (which in turn causes rise in switching losses) or using negative gate voltage to turn OFF the MOSFET or using gate drivers with active miller clamp.

Reducing Loop Inductance in Power Section & symmetric positioning of devices:

The stray inductances in power side loops cause high ringing in the switching nodes. The result is additional voltage stress on the devices and rise in losses when the loops have high dv/dt . The loop size reduction is achieved by closely placing the components (as shown in Figure 42) for AC-DC stage).

The top and bottom MOSFETs of the full bridge network are placed as close as possible. The positions are such that a straight trace connects top MOSFET source and bottom MOSFET drain pins. A ceramic capacitor for decoupling is connected directly between top MOSFET drain and bottom MOSFET source pin and closest to both to absorb the energy in stray inductance during switching. A RC snubber is also placed close to the devices to damp out oscillations caused by switching. The snubber network is placed close to both the paralleled legs with high frequency switching.

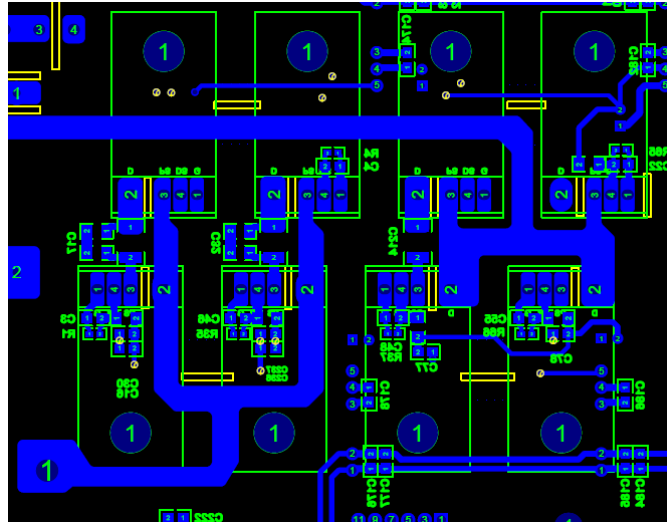


Figure 42.8 Power traces (bottom) and snubber capacitors for ac-dc stage

To minimize high frequency ripple voltage, film capacitors with values greater than the snubber capacitors are placed adjacent to each full bridge network. Electrolytic capacitor bank to reduce ripple voltage amplitude at double the line frequency is connected at a faraway distance (Can also be made as a separate board). The symmetrical layout of traces with respect to each

paralleled MOSFET need to be checked properly. This has been checked experimentally that the layout is the most important parameter in equal sharing of current under all conditions.

Minimizing EMI due to Inductor:

In the hard-switching application at higher frequencies, the parasitic capacitance of the inductor also contributes to the ringing in drain voltage. This capacitance between windings or layers of inductor and the stray inductance in power switching loop leads to ringing in drain voltage. The capacitance between adjacent windings will not have much contribution due to low voltage between them. But the dv/dt across capacitor between adjacent layers will be high enough.

A single layer winding is an ideal solution for minimizing parasitic capacitance of inductor. Sufficient insulation between inter layers of windings can also help. To minimize the radiated

noise from core, twisting the windings can be done within the core to generate a radiated flux cancellation mechanism (as shown in Figure 43).

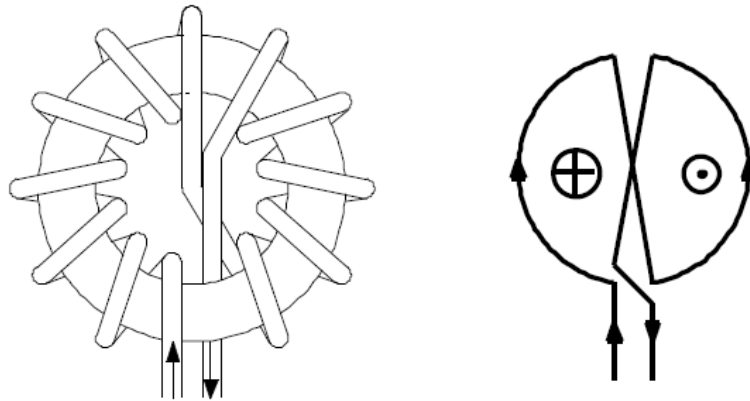


Figure 43. Winding structure to reduce radiated emission from inductor

4.2 Controller Board

The block diagram of controller card is shown in Figure 44. The controller board houses the Texas Instruments TMS320F28377 dual core Delfino microcontroller. The TMS320F2837xS is a powerful 32-bit floating-point microcontroller unit designed for advanced closed-loop control applications and suits digital power conversion. The 32-bit C28x floating-point CPU provides 200 MHz of signal processing performance. The controller supports up to 1MB of onboard flash memory with error correction code (ECC) and up to 164KB of SRAM. Two 128-bit secure zones are also available on the CPU for code protection. The peripherals include ADCs with comparator, DACs, PWMs, eCAPs, eQEPs and more.

The controller signals are galvanically isolated from the power stage. The board to board connectors are placed such that the signals from controller board to gate drivers/sensors are as short as possible. The voltages and currents to be measured are routed to the controller board through cables and terminal blocks. The supply for the controller and the on-board sensors is generated through the on-board regulators powered from external 7V supply. For the gate drivers, separate external power supply of 15V is used which is routed to the power board along with the PWM signals.

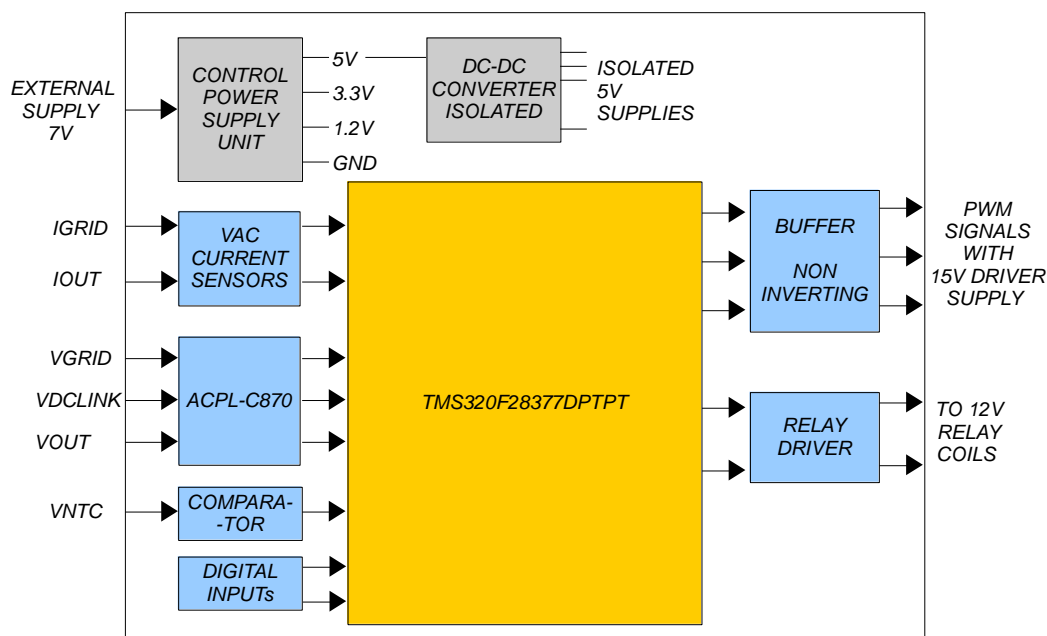


Figure 44. Controller board block diagram

4.2.1 Power Supply Requirements

Major components of the controller board that consume most of the power are: the microcontroller, the buffer ICs, analog isolation amplifiers and the VAC current sensors. An estimate of power consumption is given in Table 13.

| VOLTAGE | CURRENT | POWER | NOTES |
|---------|---------|--------|--|
| 3.3V | 0.105A | 0.35W | Maximum current on VDDIO, VDDA and VDD3VFL |
| 1.2V | 0.36A | 0.432W | Maximum current on VDD at 200MHz |
| 5V | 0.08A | 0.4W | Buffer ICs for 12PWM signals |
| | 0.08A | 0.4W | VAC sensor consumption |
| | 0.026A | 0.13W | ACPL-C780 |
| | 0.1A | 0.5W | Additional safety margin (100mA) |

Table 13. Controller board power consumption

Power Dissipation in TPS704405:

The power dissipation in the regulators is dominated by the difference in input and output voltages. The combined power loss due to both regulators is:

$$P_{reg} = (V_{IN} - V_{OUT1})I_{OUT1} + (V_{IN} - V_{OUT2})I_{OUT2}$$

$$P_{reg} = (5 - 3.3)0.105 + (5 - 1.2)0.36 = 1.55W$$

The power loss has to be dissipated to the ambient in form of heat to prevent the device thermal shutdown caused by the junction temperature rising to 150°C.

The PWP package of regulator has a thermal pad that is connected to the ground pin and hence the ground plane. The capacity can be increased if air flow is also provided to the pad. The thermal impedance for different copper area along with different airflow is shown in Figure 46. For an ambient temperature at 50°C, to limit the junction temperature to 125°C, the effective thermal resistance should be:

$$R_{thJA} = \frac{125-50}{P_{reg}} = \frac{48.4^{\circ}C}{W}$$

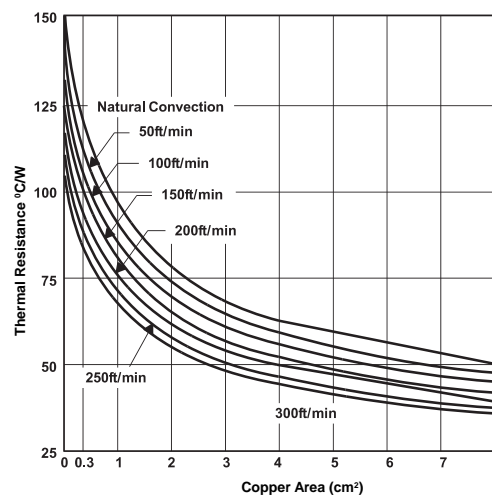


Figure 46. TPS70445 thermal resistance versus dissipation area

From the plot in Figure 46, the area copper heatsink area required to maintain junction temperature within 125°C will be around 8cm² with natural convection.

Other supplies:

1. Reference voltage to ADC pins

The reference voltage to the controller ADC pins is 3.3V. To achieve tight regulation in reference voltage and prevent any noise interference, a low drift low power precision voltage reference IC REF3230 is used (as shown in Figure 47).

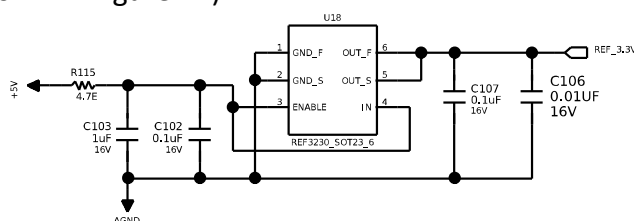


Figure 47. Generating ADC reference voltage using REF3230

The reference is stable with any capacitive load and can operate at inputs as low as 5mV above the output voltage and drive loads up to 10mA. The output voltage has a variation of +/-7mV with a drift of maximum 20ppm/°C.

2. Reference voltage for current and voltage measurements

For the VAC current sensors, an external voltage reference is provided which corresponds to the zero-current output voltage of the sensor. The ISL21010CFH315Z generates 1.5V reference with accuracy of +/-0.2%. Similarly, for the grid voltage feedback, a reference of 1V is generated by using voltage drop across 100Ω resistor into which a 10mA current through LT3092 is pumped.

3. Isolated supplies to isolation amplifiers

For all the bias voltages of the analog isolation amplifiers, an isolated DC-DC converter module B0505XT, like the one in Figure 34, is used. The power supply has a 5V input and 5V output isolated by 1.5kV. The device can support up to 200mA output and has a protection against short circuit.

4.2.2 Analog Feedbacks

All analog feedback circuitry is a part of the controller board. The voltages to be measured, grid voltage, DC bus voltage and the output voltage are brought to the board through 2 pin headers. The current sensors for grid and the output current are in the controller board with a current sensing path routed to the controller board via power cables.

Voltage Feedbacks:

The voltage feedbacks are isolated through an optically isolated voltage sensor ACPL-C780. The IC has input voltage range of 2V and 1GΩ input impedance, unity gain differential outputs with isolation of 5kV from the inputs. The input is scaled down to 2V range using resistive potential divider. The isolator outputs are followed by a differential amplifier stage (as shown in Figure 48) for the DC bus voltage feedback.

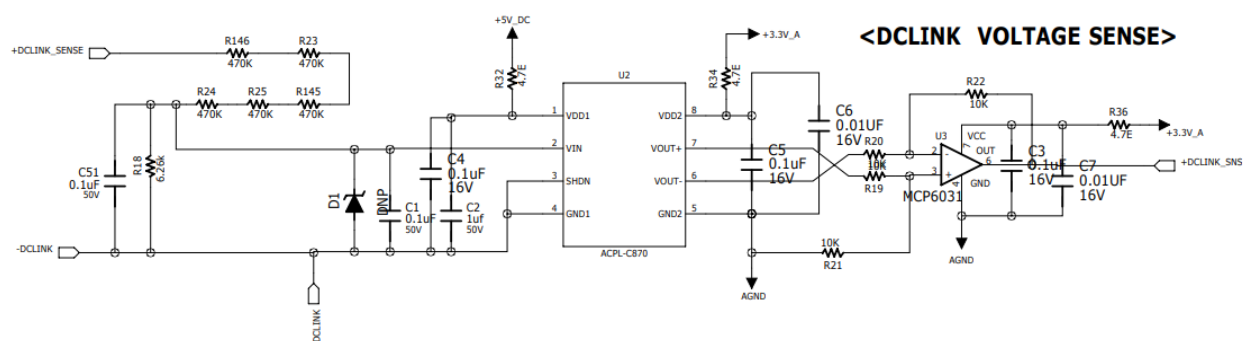


Figure 48. DC bus voltage feedback using ACPL-C780

The shutdown of amplifier is always disabled by connecting the SHDN pin to ground. The primary and secondary side supplies are decoupled by a set of ceramic capacitors close to the pins. The secondary and differential amplifier is biased with 3.3V with rail to rail op-amp. Thus, the controller pins never cross 3.3V for any magnitude of sensing voltages.

The isolation amplifier has unity gain and the differential amplifier is also designed for unity gain. The attenuation of feedback network is decided by the resistive divider network alone.

$$A_{dclink} = \frac{6.26k}{6.26k + 2350K} = 2.6567 \times 10^{-3}$$

The nominal input voltage for ACPL-C780 is 2V and full-scale input is 2.46V. For protection of the input pins, a 2.2V Zener is placed across input pins. The maximum DC bus voltage that can be sensed linearly is:

$$V_{dclink-SNS} = \frac{2.2}{A_{dclink}} = 828V$$

The DC bus voltage feedback is linear up to 2.2V, for the DC bus feedback of 882V. Beyond this value, the feedback saturates and remains at 2.2V.

Similarly, for the output DC voltage feedback, the linear sensing range is:

$$V_{out-SNS} = \frac{2.2}{A_{vout}} = 532V$$

For the grid voltage sensing, the feedback has to be level shifted to accommodate both positive and negative half of the grid voltages. A 1V stable and accurate reference is generated using LT3092 (as shown in Figure 49) and added to the grid voltage attenuation network. The constant current output generated by LT3092 is:

$$I_{out-LT3092} = \frac{10\mu R_{set}}{R_{out}} = \frac{10\mu \times 47k}{470||100||100} = 10.4mA$$

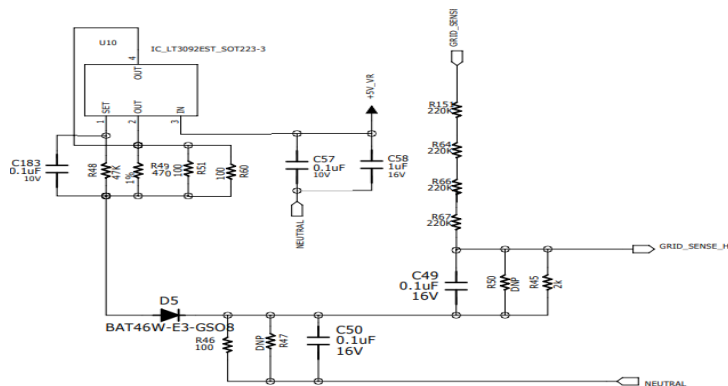


Figure 49. Generating a 1V reference voltage for grid voltage feedback

The constant current source is connected across a standard resistance of 100Ω to generate 1.0V reference (it can be adjusted accurately using a parallel tuning resistor) . The differential amplifier gain on isolation amplifier secondary is also kept at unity. With the superposition principle, the output voltage of the divider network is:

$$V_{ac-div} = 0.9977 + (V_{grid} \times 22.675 \times 10^{-4})$$

The feedback voltage for grid voltage of 0V is 0.9975V. The positive peak is clamped to 2.2V and the negative voltage to 0V. The voltage feedbacks are terminated to the ADC pins through a RC low pass filter stage placed close to the microcontroller.

Current Feedbacks:

The type of currents measured in the system are grid current, output current and the bridge current of the DC-DC converter. The grid and output current feedbacks, used for closed loop

control, system monitoring and protection, are derived from Vacuumschmelze (or VAC) T60404-N4646-X161 current sensor module. For the bridge current, a high frequency current sense transformer PE-67100NL is used.

The grid current measurement using VAC sensor is shown in Figure 50. The sensing range of sensor is 50A (RMS) nominal and 172A peak. The sensor has an internal reference of 2.5V±2.5mV for zero current output which is independent of bias voltage of 5V at VC pin. The sensor sensitivity is 12.5mV/A, however as 2 turns have been used inside the sensor, sensitivity changes to 25mv/A. External reference voltage in range of 0 to 4V can be applied to VREF pin.

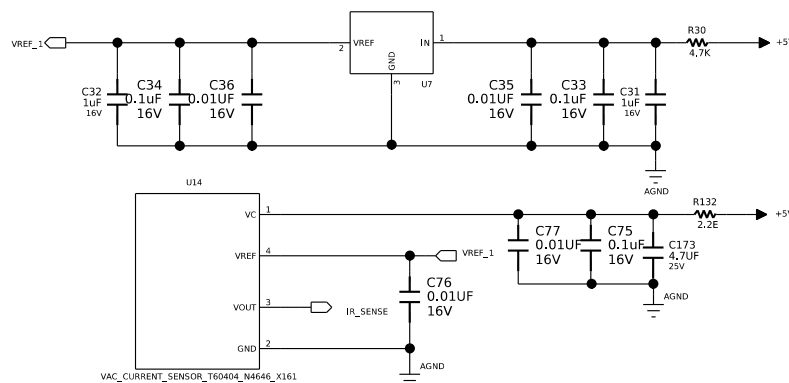


Figure 50. Grid current measurement using VAC sensor

An external reference of 1.5V is generated through ISL2101D and given to the current sensor. The new feedback voltage for 0A current is 1.5V. The negative peak current that can be sensed is:

$$I_{ac-SNS-pk} = \frac{1.5}{0.025} = 60A$$

The value of PFC peak current as computed earlier is:

$$I_{SWpk} = I_{Lmax} + \frac{\Delta I_L}{2} = \frac{6600}{200} \sqrt{2} + \frac{15}{2} = 54.17A .$$

This implies that any negative peak more than 60A shall be computed as 60A, however, the positive peak can go up to 66A for which the output voltage will be 3.3V. Software protection should work well below this value. Though the system currents cannot go to such high levels, the current has to be well within 66A for the ADC pin to be within 3.3V level. The current transformer feedback from bridge of DC-DC converter is used for the protection and the system trip, in case the current crosses a preset threshold level. The scaled down current is rectified before reaching the 10Ω burden resistance. The overcurrent protection is implemented using the internal comparators of the analog pin. The feedback voltage is 3.3V for peak input current of 33A.

4.2.3 Controller Pin Assignments

The microcontroller peripherals used in the charger system are ePWMs, ADCs and GPIOs.

PWM Pins:

The controller supports 12 ePWM modules or 24 ePWM pins with 8 submodules, that can provide HRPWM (high resolution PWM outputs). The PWM outputs can be made available at the GPIOs. The output from comparator submodule can be to the PWM trip inputs through X-BAR. In the charger, the PWM used are listed in Table 14. All PWM pins used are of high resolution type and are controlled by fault inputs scanned at GPIOs and the outputs from internal analog comparator submodules through X-BAR.

| Pin No. | Pin Name | Pin Used As | Remarks |
|---------|----------|-------------|--|
| 160 | GPIO0 | EPWM_1A | Ac-dc converter stage leg 1 top PWM signal Active high output |
| 161 | GPIO1 | EPWM_1B | Ac-dc converter stage leg 1 bottom PWM signal Active high output |
| 162 | GPIO2 | EPWM_2A | Ac-dc converter stage leg 2 top PWM signal Active high output |
| 163 | GPIO3 | EPWM_2B | Ac-dc converter stage leg 2 bottom PWM signal Active high output |
| 164 | GPIO4 | EPWM_3A | Dc-dc converter primary leg 1 top PWM signal Active high output |
| 165 | GPIO5 | EPWM_3B | Dc-dc converter primary leg 1 bottom PWM signal Active high output |
| 166 | GPIO6 | EPWM_4A | Dc-dc converter primary leg 2 top PWM signal Active high output |
| 167 | GPIO7 | EPWM_4B | Dc-dc converter primary leg 2 bottom PWM signal Active high output |
| 18 | GPIO8 | EPWM_5A | Dc-dc converter secondary leg 1 top PWM signal Active high output |
| 19 | GPIO9 | EPWM_5B | Dc-dc converter secondary leg 1 bottom PWM signal Active high output |
| 1 | GPIO10 | EPWM_6A | Dc-dc converter secondary leg 2 top PWM signal Active high output |
| 2 | GPIO11 | EPWM_6B | Dc-dc converter secondary leg 2 bottom PWM signal Active high output |

Table 14. PWM pins of the microcontroller

ADC Pins:

The controller ADC module is a successive approximation style ADC. There are 4 ADC modules with a resolution that can be selectable between 12 bits (290ns conversion) and 16 bits (915ns conversion). The ADC supports single ended and differential signals. The single ended signals are referred to VREFLO pins. The ADC triggering, and conversion sequencing is accomplished through configurable start-of-conversions (SOCs). Multiple SOCs can be configured for the same trigger, channel, and/or acquisition window as desired.

The ADC signals used in charger are listed in Table 15. All the signals are single ended with VREFHI signals connected to 3.3V and the VREFLO pins connected to VSS. All the signals have a RC filter network prior to connection to the microcontroller. The pin impedance, which is dependent on ADC clock (5MHz to 50MHz) decides the filter resistance. The pin has parasitic input capacitance of maximum 12.9pF and 117pF (for ADCINB0 due to VDAC functionality) and the filter capacitance should be at least 100 times higher.

| Pin No. | Pin Name | Pin Used As | Remarks |
|---------|----------|-------------|--|
| 31 | ADCINC2 | ADCINC2 | DCLINK_SNS: Dc bus voltage feedback |
| 38 | ADCINA5 | ADCINA5 | GRID_SNS : Grid voltage feedback |
| 40 | ADCINA3 | ADCINA3 | VOUT_SNS: Output voltage feedback |
| 44 | ADCIN14 | ADCIN14 | CT_SENSNE: Dc-dc bridge current feedback |
| 39 | ADCINA4 | ADCINA4 | IOUT_SENSE: Output current feedback |
| 49 | ADCINB3 | ADCINB3 | IR_SENSE: Grid current feedback |
| 47 | ADCINB1 | ADCINB1 | ADC reference voltage monitoring |
| 46 | ADCINB0 | ADCINB0 | NTC over-temperature feedback monitoring |

Table 15. ADC pins of the microcontroller

GPIO Pins:

The GPIOs of the controller have up to 12 independent peripheral signals multiplexed per pin along with the CPU controlled input output capability. There are 6 ports and up to 168 GPIO pins. In the charger, GPIOs are used for control of relays, indication LEDs and receive user selectable digital inputs (as listed in Table 16).

| Pin No. | Pin Name | Pin Used As | Remarks |
|---------|----------|-------------|---|
| 24 | GPIO24 | GPIO24 | For control of grid side relay to bypass charging resistor. Active high output |
| 23 | GPIO23 | GPIO23 | For control of output side relay (Not mounted) Active high output |
| 142 | GPIO76 | GPIO76 | Indication / debug LED 1 Active high output |
| 143 | GPIO77 | GPIO77 | Indication / debug LED 2 Active high output |
| 144 | GPIO78 | GPIO78 | Indication / debug LED 3 Active high output |
| 145 | GPIO79 | GPIO79 | Indication / debug LED 4 Active high output |
| 131 | GPIO43 | GPIO43 | Control switch: for ON/OFF control Active high / low output (settable) |
| 134 | GPIO70 | GPIO70 | Control switch: for charging/ inverter mode selection Active high / low output (settable) |

Table 16. GPIO pins of the microcontroller

5. Performance Data



CAUTION

HIGH VOLTAGE RISK

THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS BOARD WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS BOARD CAN REACH TEMPERATURES ABOVE 50° CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED. DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD.

The connectors on the board have very high voltage levels present when the board is connected to an electrical source, and thereafter until the bulk capacitors are fully discharged. Please ensure that appropriate safety procedures are followed when working with these connectors as serious injury, including death by electrocution or serious injury by electrical shock or electrical burns, can occur if you do not follow proper safety precautions. When devices are being attached for testing, the board must be disconnected from the electrical source and all bulk capacitors must be fully discharged. After use the board should immediately be disconnected from the electrical source. After disconnection any stored up charge in the bulk capacitors will continue to charge the connectors. Therefore, you must always ensure that all bulk capacitors have completely discharged prior to handling the board.

警告

高压危险

接通电源后，该评估板上可能存在非常高的电压，板子上一些组件的温度可能超过 50 摄氏度。此外，移除电源后，上述情况可能会短暂持续，直至大容量电容器完全释放电量。通电时禁止触摸板子，应在大容量电容器完全释放电量后，再触摸板子。

板子上的连接器在充电时以及充电后都具有非常高的电压，直至大容量电容器完全释放电量。请确保在操作板子时已经遵守了正确的安全流程，否则可能会造成严重伤害，包括触电死亡、电击伤害或电灼伤。连接器件进行测试时，必须切断板子电源，且大容量电容器必须释放了所有电量。使用后应立即切断板子电源。切断电源后，大容量电容器中存储的电量会继续输入至连接器中。因此，必须始终在操作板子前，确保大容量电容器已完全释放电量。

警告

高压危险

通电してから、ボードにひどく高い電圧が存在している可能性があります。ボードのモジュールの温度は50度以上になるかもしれません。また、電源を切った後、上記の状況がしばらく持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。通电している時にボードに接触するのは禁止で

す。大容量のコンデンサーで電力をまだ完全に釈放していない時、ボードに接触しないでください。ボードのコネクターは充電中また充電した後、ひどく高い電圧が存在しているので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。ボードを操作している時、正確な安全ルールを守っているのを確保してください。さもないければ、感電、電撃、厳しい火傷などの死傷が出る可能性があります。設備をつないで試験する時、必ずボードの電源を切ってください。また、大容量のコンデンサーで電力を完全に釈放してください。使用后、すぐにボードの電源を切ってください。電源を切った後、大容量のコンデンサーに貯蓄している電量はコネクターに持続的に入るので、ボードを操作する前に、必ず大容量のコンデンサーの電力を完全に釈放するのを確保してください

CPWR-AN24, Rev -, 06-2018

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The completely assembled system (as shown in Figure 51) of Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger is tested at the load conditions that are listed in the Table 2. The individual converters are independently tested for functionality and performance. The cascaded system is also tested for full load range and the results are presented in this section.

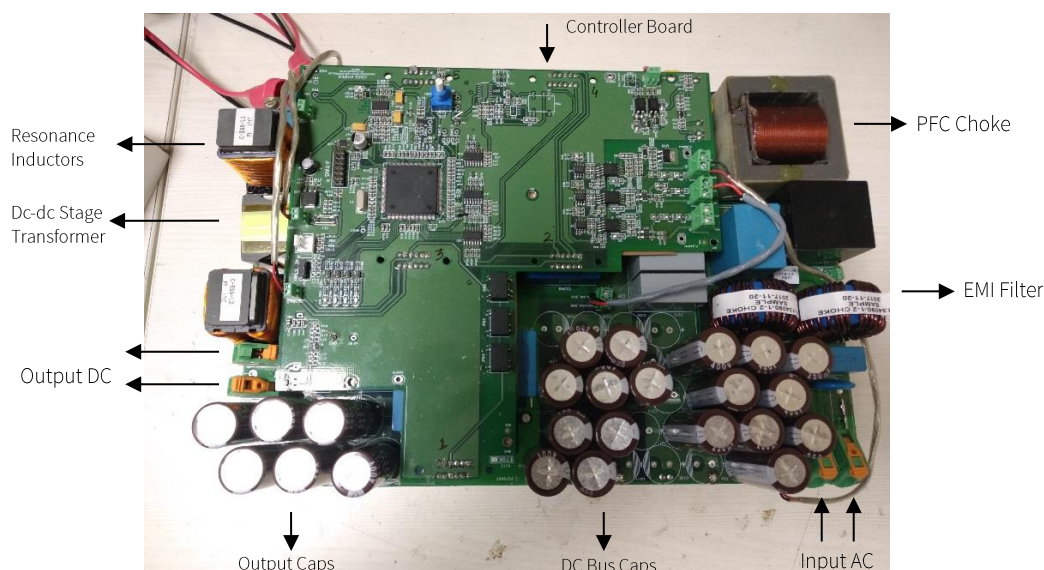


Figure 51. Cree's CRD-06600FF10N, 6.6 kW Bi-Directional EV On-board Charger (Fully Assembled)

AC-DC STAGE:

The AC-DC stage has nominal output voltage of 390V but can go up to 680V for operating DC-DC stage at resonant frequency. One of the legs has switching frequency of 67kHz. The gate voltage (yellow) and drain to source voltage (green) are shown in Figure 52, (for the DC link voltage of 680V and the gate resistance of 10Ω). There is no ringing or oscillations observed in the gate voltage. The waveforms of the MOSFETs used for synchronous rectification and the zero-voltage switching can be seen at turn ON and turn OFF



Figure 52. High frequency MOSFET's Gate Voltage (Yellow) and Drain to Source voltage (Green) during turn ON and turn OFF

The top and bottom MOSFETs are switched with complementary gate pulses with adequate dead-time. The top and bottom MOSFET voltages (yellow and green) of high frequency switching leg at 680V output along with the inductor current (pink) are shown in Figure 53. There is no peak overshoot or sever ringing in the drain source voltage during turn OFF.

The grid voltage (Blue) and inductor current (Pink) for 1.4kW and 6kW power are shown in Figure 54. At 1.4kW load, the current drawn from grid was 6.25A and the current THD was 10.736%. In both the cases, the inductor current waveform closely follows the grid voltage. At 6kW load, the grid current was 26.73A with a THD of 6.37%. In both the cases, the output voltage was set to 680V.



Figure 53. Top and Bottom MOSFET Voltages (Yellow and Green) along with the inductor Current (Pink)

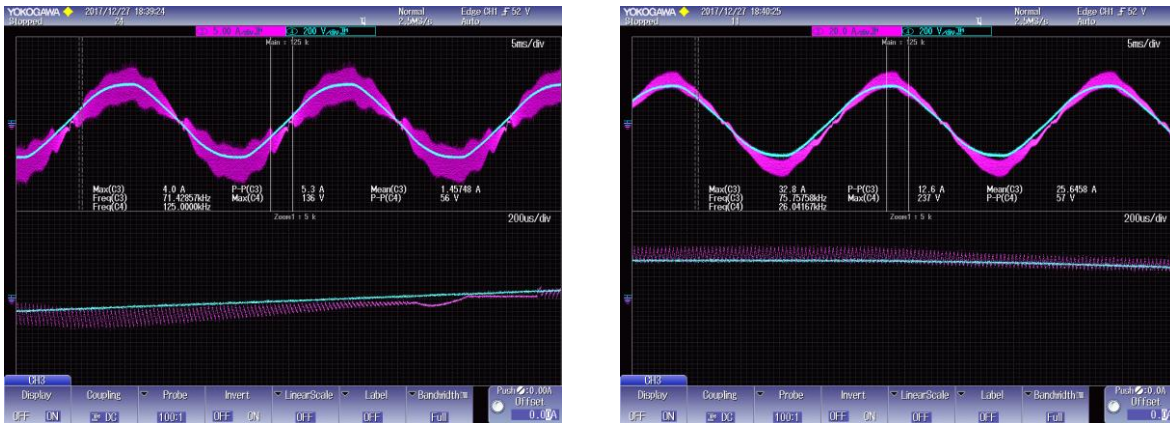


Figure 54.9 Grid voltage (Blue) and inductor Current (Pink) at 1.4kW and 6kW

The measured efficiency of the AC-DC stage including the input EMI filter for 390V and 680V output over the entire load range are shown in Figure 55. In both the cases, the peak efficiency is maintained close to 98%.

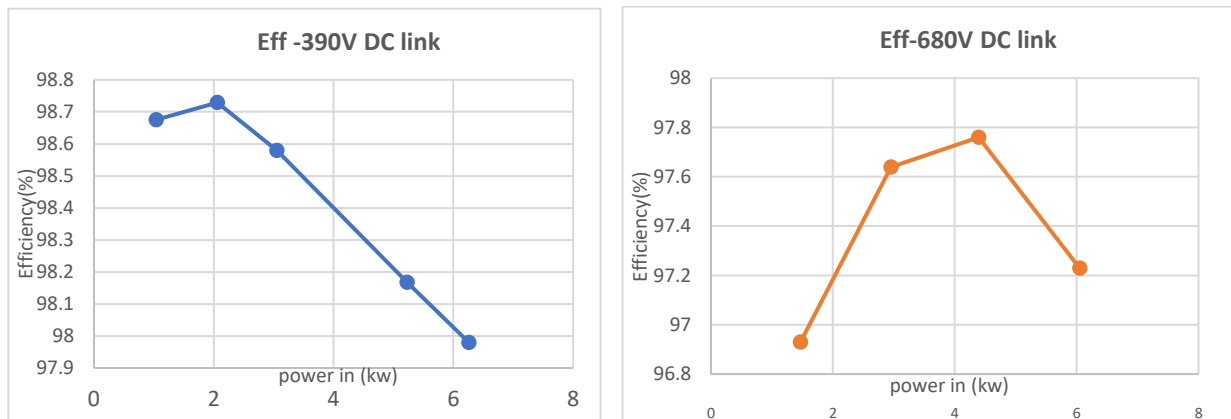


Figure 55. AC-DC Converter measured efficiency at 390V and 680V DC link Voltages

DC-DC STAGE

The DC-DC converter is tested with resistive load and for output voltage regulation. The input voltage is varied to make the converter operate close to resonance frequency and attain the required gain. The primary current (pink) and the primary MOSFET gate (green) and drain source (yellow) voltages at no load are shown in Figure 56. The three waveforms at full load for 280V (limited to 4.5kW) output and 450V output (at 6.2kW) are shown in Figure 57.



Figure 56. Primary Current (Pink), MOSFET Gate (Green) Voltage and Drain to Source (yellow) Voltage at no load

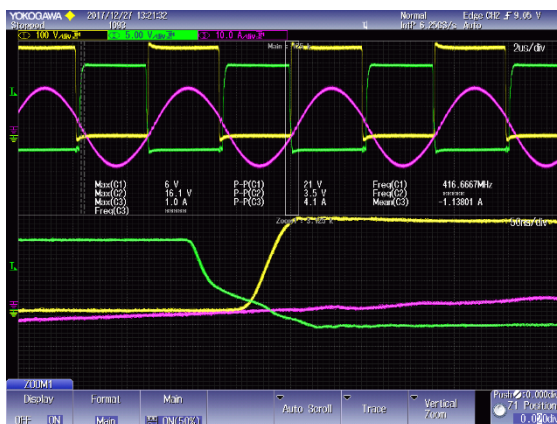


Figure 57. Primary Current (Pink), MOSFET Gate (Green) Voltage and Drain to Source Voltage (Yellow) at 260V and 450V Output

The measured DC-DC converter efficiency with resistive load at 260V and 450V outputs over entire load range is shown in Figure 58.

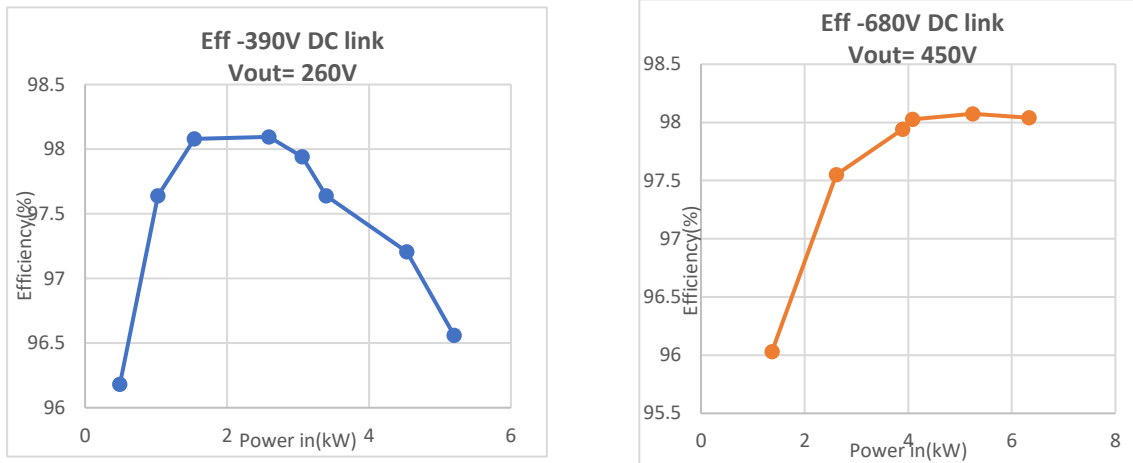


Figure 58. DC-DC Converter Efficiency at 260V and 450V Output Voltages

CASCADED SYSTEM:

The total system is powered up with 230V grid input. The DC output reference is set to 260V and loaded to 4.3kW. The input voltage and current waveforms and the power analyzer readings for input and output are shown in Figure 59. Similarly, the waveforms and power analyzer readings for 450V, 6.6kW output are shown in Figure 60.

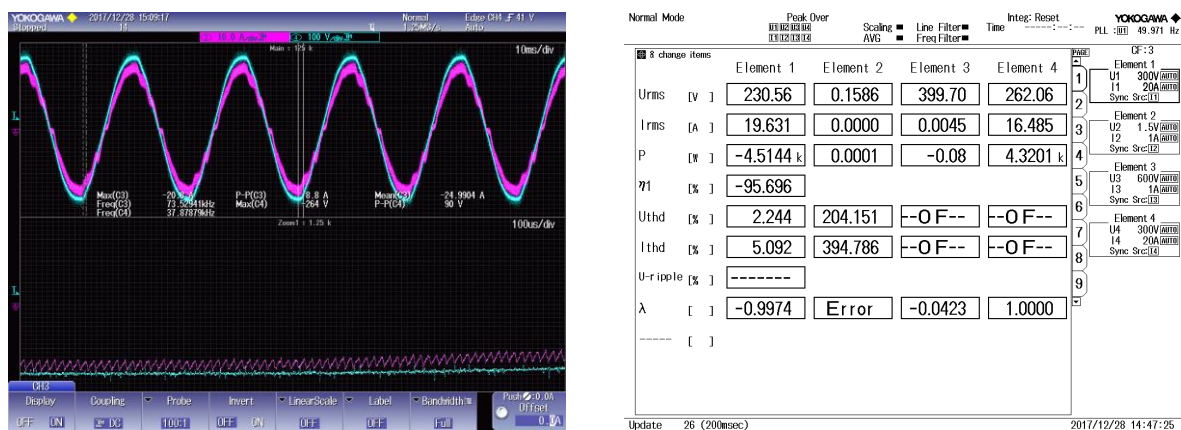


Figure 59. Grid Voltage (Blue) and Current (Pink) Waveforms and Power Analyzer readings for 260V output

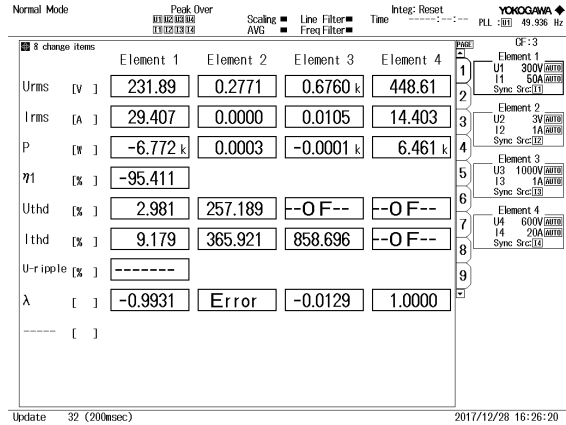


Figure 60. Grid Voltage (Blue) and Current (Pink) Waveforms and Power Analyzer readings for 450V output

The efficiency for 260V and 450V outputs at various loading conditions is shown in Figure 61.

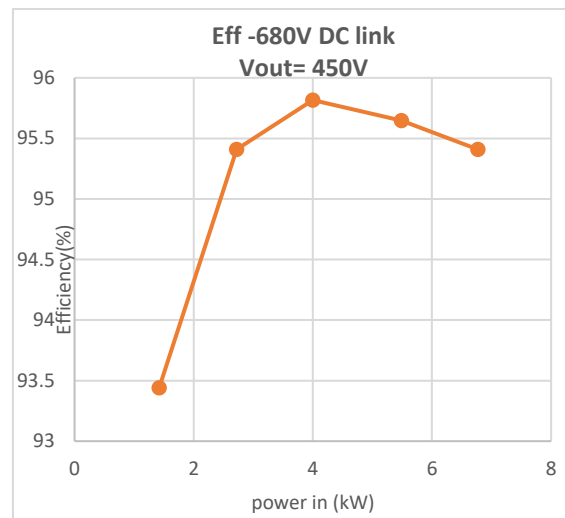
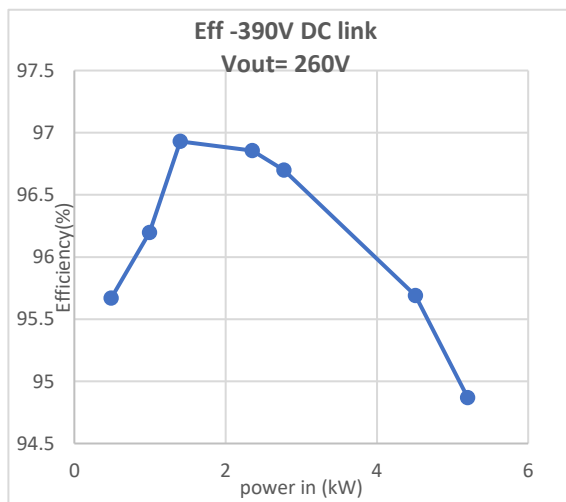
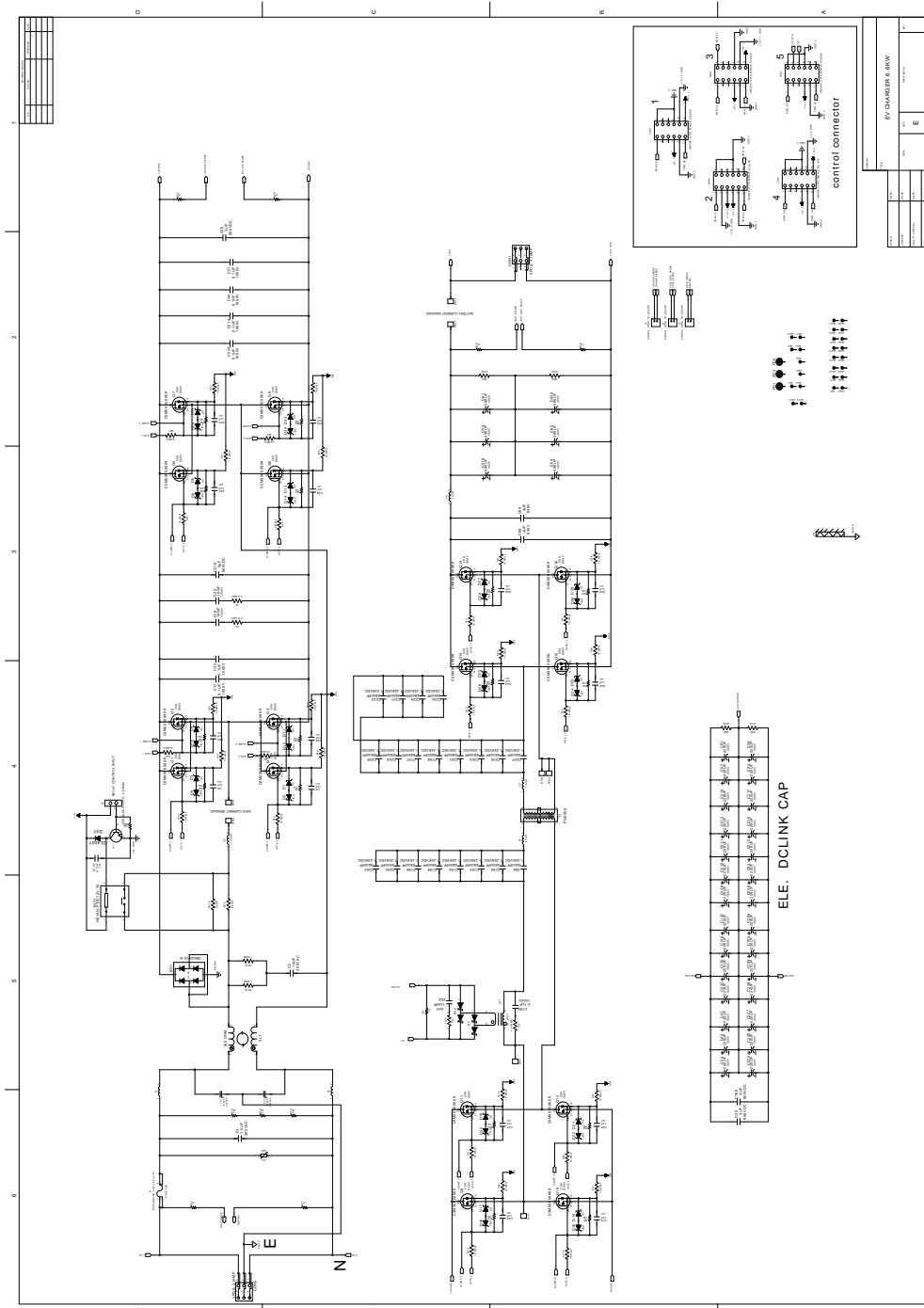


Figure 61. Charging mode efficiency at two 260V and 450V output voltages

6. Appendix

Power Board Schematics:



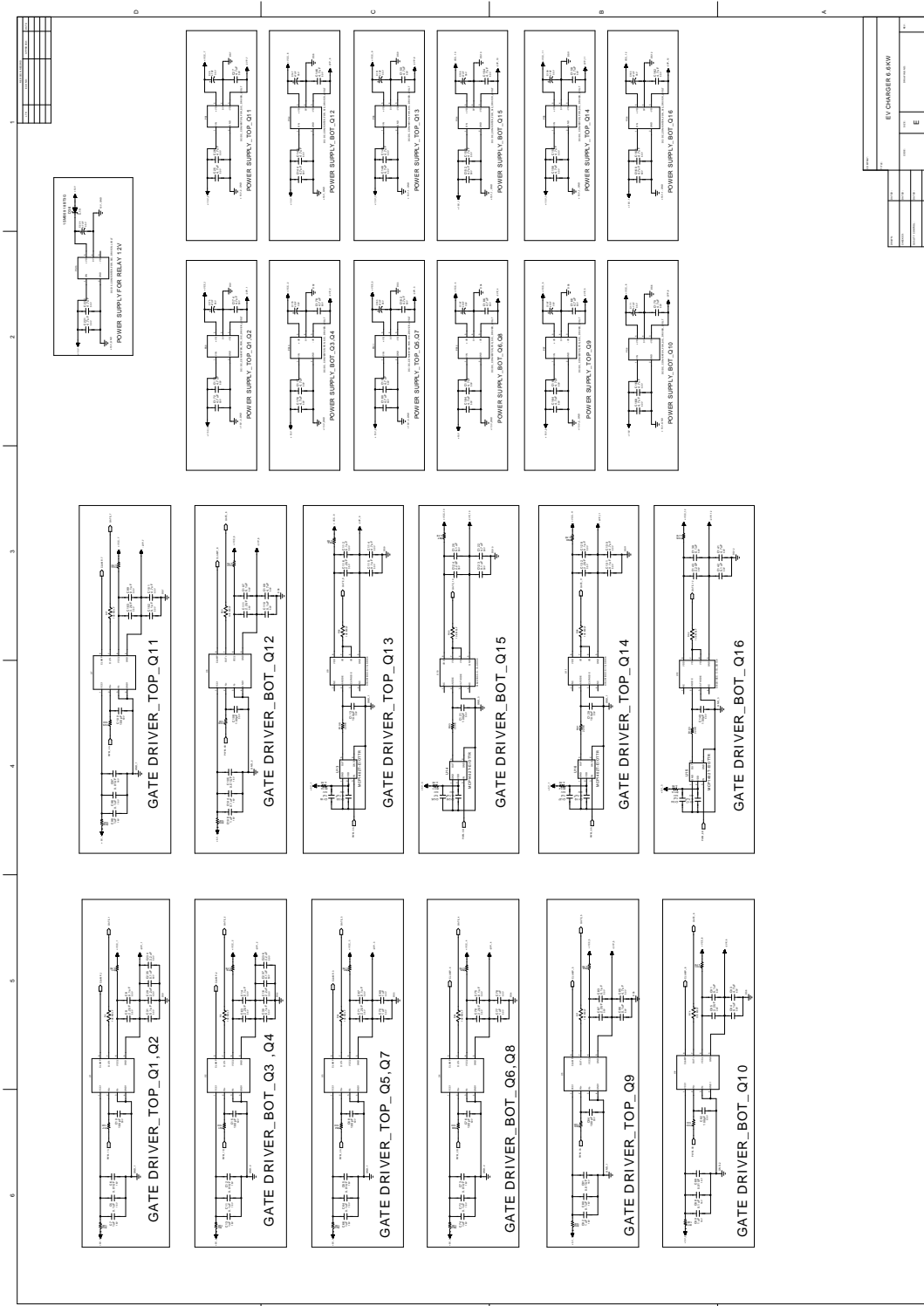
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Power Board Page 2:



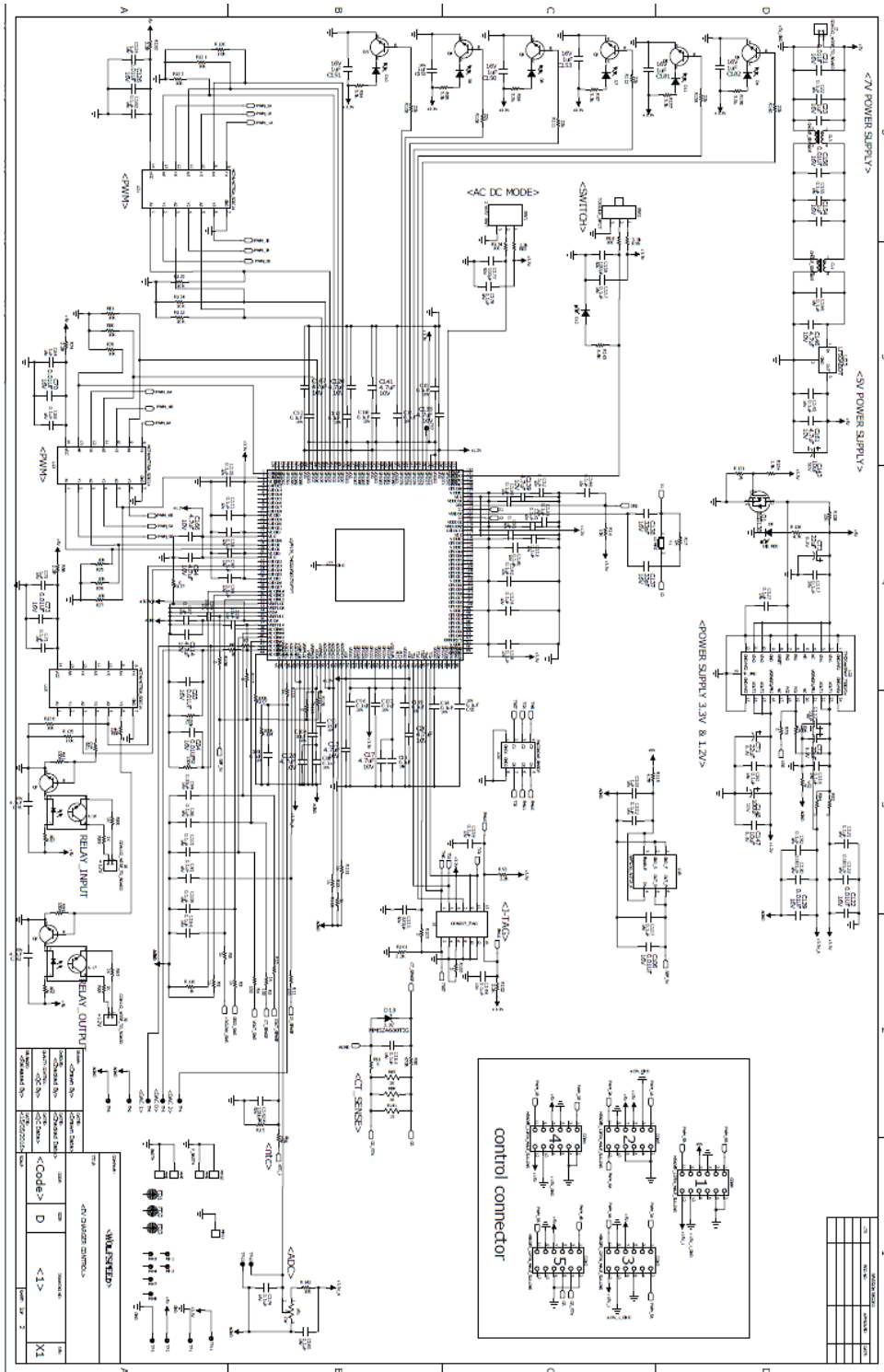
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Control Board Schematic:

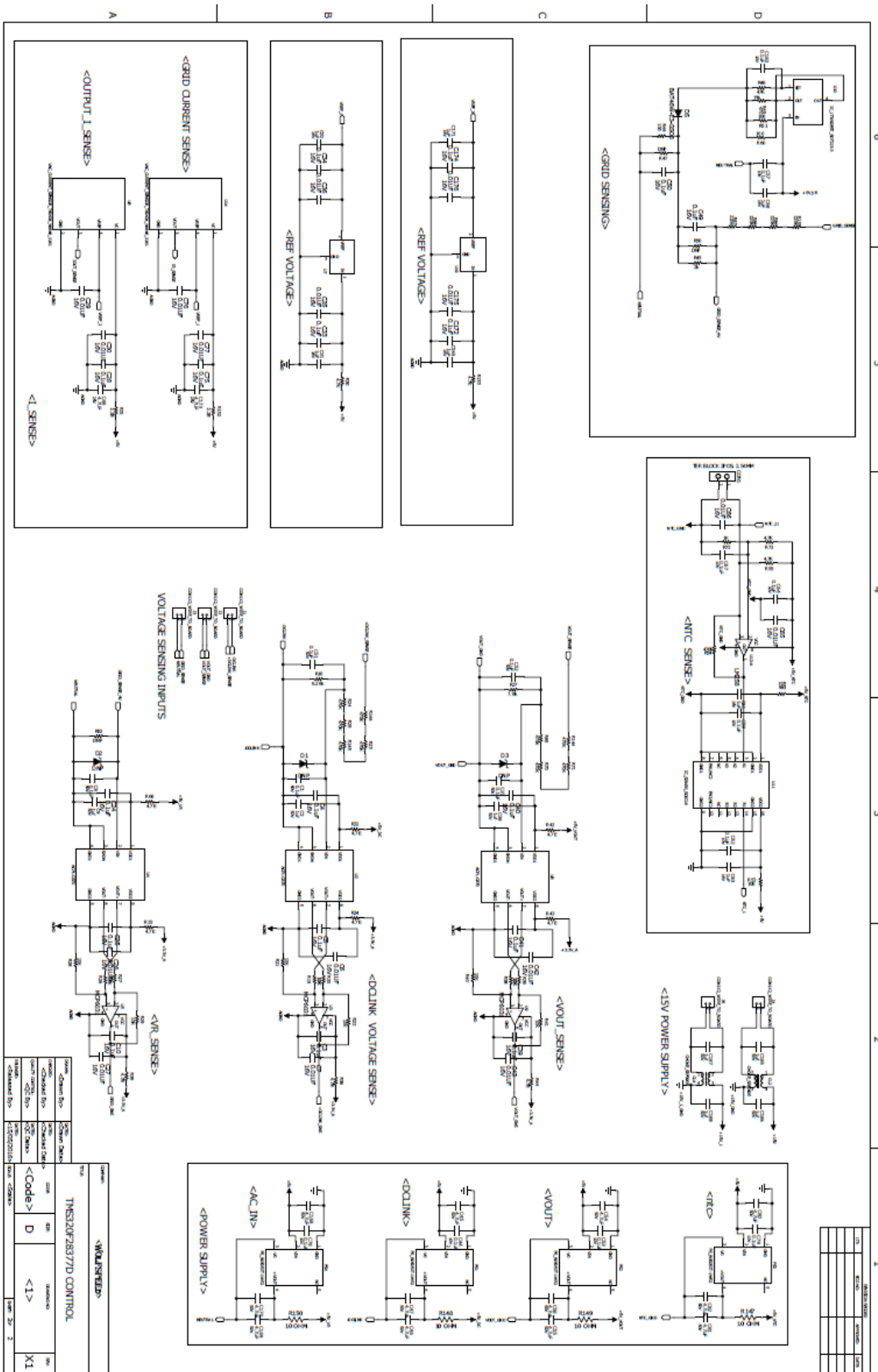


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BILL OF MATERIALS:

Power Board:

| Sr No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|-------|-----|--|--------------------------------------|--------------|---------------------|---------|
| 1 | 1 | BD1 | BRIDGERECT SINGLE PHASE 1000V 25A TH | COMCHIP | GBU2510-G_DNP | TH |
| 2 | 8 | C6 C12 C65 C73 C81 C89 C97 C105 | CAP CER 0.01UF 10% 16V X7R 0603 | TDK CORP. | C1608X7RIC103K | CAP0603 |
| 3 | 8 | C5 C11 C64 C72 C80 C88 C96 C104 | CAP 0.1uF 10% 16V X7R 0603 | KEMET | C0603X104K4 RACTU | CAP0603 |
| 4 | 16 | C8 C14 C67 C75 C83 C91 C99 C107 C112 C117 C119-120 C126 C128 C133 C139 | CAP CER 0.1uF 10% 50V X7R 0603 | KEMET | C0603C104K5 RACTU | CAP0603 |
| 5 | 8 | C7 C13 C66 C74 C82 C90 C98 C106 | CAP CER 1.0uF 10% 16V X5R 0603 | KEMET | C0603C105K4 PACTU | CAP0603 |
| 6 | 4 | C118 C125 C127 C134 | CAP CER 1uF 10% 50V X7R 0603 | PANASONIC | CL10A105KB8NNNC | CAP0603 |
| 7 | 12 | C9 C63 C71 C79 C87 C95 C103 C111 C116 C124 C132 C143 | CAP0603 2.2UF 35V X5R | MURATA | GRM188R6YA225KA12D | CAP0603 |
| 8 | 12 | C30-31 C86 C94 C102 C110 C115 C123 C131 C142 C226 C228 | CAP CER 0.1uF 10% 50V X7R 0805 | TDK | C0805C104K5 RAC7410 | CAP0805 |
| 9 | 1 | C62 | CAP0805 100PF 50V | | | CAP0805 |
| 10 | 16 | C3-4 C19-20 C22 C37-38 C42-43 C45-50 C55 | CAP CER 1nF 10% 50V X7R 0805 | MURATA | C0805C102K5 RACTU | CAP0805 |
| 11 | 4 | C69-70 C77-78 | CAP CER 1uF 10% 50V X7R 0805 | MURATA | | CAP0805 |
| 12 | 4 | C16 C29 C225 C227 | CAP CER 2.2uF 10% 50V X7R 0805 | MURATA | GRM32ER71H225KA88L | CAP0805 |

| Sr No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|-------|-----|--|---|--------------------|------------------------|---|
| 13 | 47 | C25-27 C34 C40 C85 C93 C101 C109 C114 C122 C130 C141 C144-146 C148-150 C152-154 C156-158 C160-162 C164-166 C168-170 C172-174 C176-178 C180-182 C184-186 C191 | CAP CER 4.7uF 10% 50V X7R 0805 | MURATA | GRM32ER71H 475KA88L | CAP0805 |
| 14 | 2 | C18 C33 | CAP CER 10000PF 10% 1000V X7R 1206 | MURATA | GRM31CR73A 103KW03L | CAP1206 |
| 15 | 4 | C17 C32 C51-52 | CAP CER 1812 0.01UF 1000V COG/NPO | KEMET | C1812C103JD GACAUTO | CAP1812 |
| 16 | 1 | C189 | CAP CER 1812 0.1UF 1000V X7R | KEMET | C1812C104K DRAC7800 | CAP1812 |
| 17 | 2 | C21 C44 | CAP CER 1812 DNP | KEMET | DNP | CAP1812 |
| 18 | 20 | C23-24 C135-138 C193 C195 C204 C210-219 C224 | CAP ELECT 220uF 400V DC RADIAL | RUBYCON | 400BXW220M EFR18X50 | DIA- 18MM, LEAD SPACE- 7.5MM, H- 50 |
| 19 | 1 | C54 | CAP ELECT 390uF 500V DC RADIAL | united chemicon | VLXS501VSN3 91MA50S | DIA-35MM, LEAD- 10MM, H- 52.5MM |
| 20 | 1 | C1 | FILM CAPACITOR 1.5UF 305VAC | EPCOS | B32923C3155 M | CAPFILM_ 26.5X12M M P- 22.5MM H- 22mm |
| 21 | 1 | C2 | FILM CAPACITOR 10UF 20% 305VAC RADIAL | EPCOS | B32926H3106 M | CAPFILM_ 42MMX28 MM P- 37.5MM H- 42.5mm |

| Sr No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|-------|-----|--|--|-----------------------|------------------------|---|
| 22 | 3 | C35-36 C188 | CAPFILM 3UF 900VDC 5% RADIAL | VISHAY BC COMP. | MKP1848530 094K2 | CAPFILM_ 15MMX32 MMX25MM , P-27.5MM |
| 23 | 30 | C39 C53 C56 C60-61 C190 C192 C194 C196-203 C205-209 C220-223 C229-233 | CAPFILM 4700pPF 10% 1.25KVDC RADIAL | EPCOS | B32651A7472 K000 | CAPFILM 13MMX5M M P=10MM ,H-11MM |
| 24 | 2 | C58-59 | FILM CAPACITOR 4UF 630V | VISHAY | B32794D2405 K | CAPFILM_ 11/315MM |
| 25 | 2 | YC1-2 | CAP CERMIC 4700PF 440VAC RADIAL | KEMET | C947U472MZ VDBA7317 | DIA 11MM P-7.50MM |
| 26 | 13 | C28 C41 C147 C151 C155 C159 C163 C167 C171 C175 C179 C183 C187 | CAP 47UF 35V ELECT PW RADIAL | PANASO NIC | ECA-1VM470I | 5/2.5MM TH |
| 27 | 1 | C57 | CAP FILM 5UF 900VDC 5% RADIAL | KEMET | C4AE0BU450 0A11J | CAP_FILM _19X31.5M Mx29.2MM P-27.5MM |
| 28 | 4 | J1-4 | CONN.TERM BLOCK 2POS. 5MM PCB | PHOENIX CONTACT | 1935161 | TH_5MM |
| 29 | 1 | CON5 | CONN TER BLOCK 3POS. 7.5MM 41AMP 30DEG | PHOENIX CONTACT | 1792232 | 3POS. 7.5MM |
| 30 | 1 | CT1 | xfrmr current sense 37a 20mh t/h | PULSE | PE-67300NL | TH |
| 31 | 13 | PS1-13 | DC/DC Converter for SiC Driver low voltage | MORNSO N | QA15115R2 | SIP PACK |
| 32 | 12 | C10 C15 C68 C76 C84 C92 C100 C108 C113 C121 C129 C140 | CAP CER 100pF 10% 50V X7R 0603 | VISHAY/V ITRAMON | VJ0603Y101K XACW1BC | CAP0603 |

| Sr No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|-------|-----|--|--|-------------------|-------------------|------------------------|
| 33 | 16 | D2 D4 D6 D10 D12 D14 D16 D18 D20 D22 D24 D26 D28 D30 D32 D34 | DIODE BZX-384-C16,115 ZENER 16V | NXP Semiconductor | BZX384-C16,115 | SOD-323 |
| 34 | 16 | D1 D3 D5 D9 D11 D13 D15 D17 D19 D21 D23 D25 D27 D29 D31 D33 | DIODE BZX-384-C3V0,115 ZENER 3V | NXP SEMI | BZX-384-C3V0,115 | SOD-323 |
| 35 | 1 | D8 | DIODE STANDARD 1000V 1A MELF | DIODES INC. | DL4007-13- | MELF |
| 36 | 2 | D7 D35 | DIODE SCHOT BAT754S 30V SOT23 | NEXPERIA USA | BAT754S,215 | SOT23 |
| 37 | 1 | D36 | DIODE ZENER 1W 2.1V SMB | ON Semiconductor | | SMB |
| 38 | 1 | XL1 | EMI 2 LINE COOMON MODE CHOKE TH 160 OHM@100MHZ 75A | LAIRD | CM5441Z101 B-10 | TH |
| 39 | 1 | F2 | FUSE 15A LEADED CARTRIDGE | LITTLE FUSE | 0217015.MXEP | TH |
| 40 | 1 | F1 | FUSE HOLDER CLIP 30A 315V | LITTLE FUSE | 0122 0093 | FUSE CLIP |
| 41 | 5 | CON2-4 CON6-7 | HEADER 12POS 2.54 pitch DUAL T-HOLE | SULLINS CONN. | EBC06DRXH | CON2X6 |
| 42 | 1 | HS1 | HEAT SINK 6.6KW | | | |
| 43 | 8 | U1-8 | IC Single Channel IGBT Gate Driver 1200V PG-DSO-8 | INFINEON TECH. | 1EDI30I12MH XUMA1 | PG-DSO-8 |
| 44 | 4 | U13-16 | IC MOSFET DRIVER 500MA SOT-23-5 | MICROCHIP | MCP1402T-E/OTTR | SOT-23-5 |
| 45 | 1 | L3 | INDUCTOR 150UH 40AMP | COIL WINDING | EK55246-341M-40AH | 58MMX58MM, H-35MM |
| 46 | 1 | L4 | INDUCTOR FIXED 12UH 19A 4.3 MOHM | | | SMD_35X2 8.6MM, H-47MM |

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| Sr No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|-------|-----|---------------------------------------|---|---------------------------|------------------------|--|
| 47 | 1 | L6 | INDUCTOR_FIXED_1 80NH_65A_0.15MOH M_SMD | WURTH ELE. | 7443082018A | SMD_10X8 MM, H-MM |
| 48 | 1 | L5 | INDUCTOR FIXED 7.6UH 20A 3.5 MOHM | | | 35MMX28. 6MM, H- 43MM |
| 49 | 2 | L1-2 | INDUCTOR TORRIOD POWER 20UH 40A TH | MICROM ETALS | OP-134090-2 | 36MM DIA,W- 21MM |
| 50 | 1 | Q17 | TRANS MMBT2222A GP NPN SOT23 | FAIRCHIL D | MMBT2222A | SOT23 |
| 51 | 16 | Q1-16 | MOSFET N-CHAN 900V 20A TO-247-3 | CREE SEMICON DUCTOR | C3M0065090 K | TO-247 |
| 52 | 1 | VRV1 | MOV VERISTOR510V 10KA DISK 20MM | EPCOS | B72220S2321 K101 | TH HOLE 20mm dia, 27mm hight 10mm pitch |
| 53 | 2 | CON1 CON8 | PCB TERMINAL BLOCK SINGLE POS | PHOENIX CONTAC T | PLA5/1-7 5- 1792216 | SINGLE POS. |
| 54 | 2 | RV1-2 | PTC RESET FUSE 440V 86MA RADIAL | APCOS | B59751C0120 A070 | TH_13MM X7.5MM, H- 18MM RAD |
| 55 | 1 | RLY1 | RELAY GEN PURPOSE 12V 40A SPST | TE CONN. | T9VV1K15- 12S | RELAY12V _TH_40A |
| 56 | 8 | R17 R21 R62 R96 R99 R102 R105 R108 | RES 100 Ohm 1% 1/10W 0603 | Vishay/D ale | CRCW060310 0RFKEA | RES0603 |
| 57 | 8 | R3 R10 R23 R63 R70 R73 R76 R79 | RES 10.0 OHM 0.1% 1/10W 0603 | Vishay/D ale | TNPW060310 R0BEEA | RES_0603 |
| 58 | 8 | R1 R9 R32 R35 R37 R47 R50 R66 | RES 10k 1% 1/10W 0603 | PANASO NIC | ERJ- 3GEYJ103V | RES0603 |

| Sr No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|-------|-----|---|------------------------------------|--------------|---------------------|--------------------|
| 59 | 8 | R36 R20 R4 R48-49 R34 R65 R16 | RES 10k 1% 1/10W 0603 | PANASONIC | ERJ-3GEYJ103V | RES0603 |
| 60 | 4 | R91 R93 R103 R109 | RES0603 220E 1% 1/10W | PANASONIC | ERJ-3GEYJ221V | RES0603 |
| 61 | 16 | R11 R19 R61 R84 R87 R90 R95 R98 R101 R104 R106-107 R110- 113 | RES 4.7E 1% 1/10W 0603 | YAGEO | RC0603JR-074R7L | RES0603 |
| 62 | 1 | R78 | RES0805 100E 5% SMD | PANASONIC | ERJ-6GEYJ101V | RES0805 |
| 63 | 1 | R69 | RES0805 100E 5% SMD | PANASONIC | ERJ-6GEYJ103V | RES0805 |
| 64 | 6 | R22 R25-29 | RES 0.0 OHM 1/10W 5% 1206 | PANASONIC | ERJ-8GEY0R00V | RES1206 |
| 65 | 1 | R7 | RES1206 1K 1% 1/4W | PANASONIC | ERJ-8GEYJ102V | RES1206 |
| 66 | 6 | R12 R14-15 R57 R59 R114 | RES 1.0M 1% 1/4W 1206 | VISHAY/DAL | CRCW12061M00FKEA | RES1206 |
| 67 | 12 | R2 R5 R24 R64 R71 R74 R77 R80 R82 R85 R88 R92 | SURFACE MOUNT RESISTOR 10E MELF | YAGEO | MMA02040C1008FB300 | 3.5X1.4MM |
| 68 | 31 | R8 R13 R18 R30 R33 R39-46 R51-54 R58 R60 R67-68 R81 R83 R86 R89 R94 R97 R100 R115-117 | RES SMD 1 OHM 1% 1/4W MELF | VISHAY | MMA02040C1008FB300 | 3.5X1.4MM 1206 |
| 69 | 1 | R38 | RES SMD 1 OHM 1% 1/4W MELF | VISHAY | MMA02040C1008FB300 | 3.5X1.4MM 1206 |
| 70 | 3 | R6 R31 R75 | RES SMD 4.7 OHM 1% 1/4W MELF | VISHAY | MCFRFTDV4R70 | 3.5X1.4MM _1206 |
| 71 | 2 | R72 R118 | RES 1.00 Ohm 5% 2W AXIAL | TE CONN. | ROX2SJ1R0 | RES_AXIAL _2W |
| 72 | 2 | R55-56 | RES 270K Ohm 5% 3W | YAGEO CORP. | FMP300JR-73-270K-ND | RES_270K _3W |

| Sr No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|-------|-----|-----------|--|-----------------|--------------------|---------------|
| 73 | 4 | U9-12 | DGTL ISOLATED GATE DRIVER 3.75KV SOIC8 | SILICON LABS | Si8261BCC-C- IS | SOIC8 |
| 74 | 1 | T1 | TRANSFORMER PQ5050 | | | 50MMX50 MM |

Controller Board:

| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|--------|-----|---|---|-----------------|---------------------|---------|
| 1 | 3 | U2 U4 U8 | Precision Optically Isolated Voltage Sensor | AVAGO TECH | ACPL-C870 | SO-8 |
| 2 | 1 | Q1 | MOSFET N- CH BSS138 220MA SOT23 | FAIRCHILD SEMI. | BSS138 | SOT23 |
| 3 | 2 | C123 C130 | CAP CER 0.001UF 10% 16V X7R 0603 | KEMET | C0603C102R4R ACT | CAP0603 |
| 4 | 26 | C6-7 C21 C26-27 C29- 30 C35-36 C42-43 C65- 66 C70 C73 C76-77 C83- 84 C106 C122 C126 C129 C156 C175-176 | CAP CER 0.01UF 10% 16V X7R 0603 | TDK CORP. | C1608X7RIC10 3K | CAP0603 |

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| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|--------|-----|--|----------------------------|--------------|-------------------|---------|
| 5 | 42 | C11-12 C14-16 C18-19 C44 C53 C57 C59 C62 C64 C67 C78-79 C85 C87-88 C93 C95-98 C100 C105 C111-113 C116 C119 C124 C131-134 C136 C140 C144 C149 C159 C183 | CAP 0.1uF 10% 10V X7R 0603 | KEMET | C0603C104K8R ACTU | CAP0603 |
| 6 | 31 | C3-5 C10 C22 C24-25 C28 C33-34 C39-41 C49-50 C60 C68 C71 C75 C92 C102 C107 C121 C145 C155 C157 C160 C172 C174 C178 C184 | CAP 0.1uF 10% 16V X7R 0603 | KEMET | C0603X104K4R ACTU | CAP0603 |
| 7 | 4 | C101 C179-180 C91 | CAP 0.1uF 10% 16V X7R 0603 | KEMET | C0603X104K4R ACTU | CAP0603 |
| 8 | 5 | C86 C99 C108 C163-164 | CAP 0.1uF 10% 16V X7R 0603 | KEMET | C0603X104K4R ACTU | CAP0603 |

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| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|--------|-----|---|---|---------------------|-----------------------------|---------|
| 9 | 3 | C117-118 C127 | CAP 0.1uF 10% 25V X7R 0603 | KEMET | C0603X104K3R ACTU | CAP0603 |
| 10 | 5 | C1 C8 C37 C51-52 | CAP CER 0.1uF 10% 50V X7R 0603 | KEMET | C0603C104K5R ACTU | CAP0603 |
| 11 | 3 | C158 C177 C142 | CAP CER 100pF 10% 50V X7R 0603 | VISHAY/VITRAMO N | 77- VJ0603Y101KX ACBC | CAP0603 |
| 12 | 4 | C89-90 C104 C109 | CAP CER 10uF 10% 10V X5R 0603 | MURATA | GRM188R61A1 06KE69D | CAP0603 |
| 13 | 19 | C23 C150- 151 C153- 154 C181- 182 C31-32 C58 C61 C63 C69 C72 C103 C125 C152 C165 C171 | CAP CER 1.0uF 10% 16V X5R 0603 | KEMET | C0603C105K4P ACTU | CAP0603 |
| 14 | 7 | C2 C9 C38 C185-188 | CAP CER 1uf 10% 50V X7R 0603 | PANASONIC | CL10B105K8N NNC | CAP0603 |
| 15 | 1 | C115 | CAP CER 330pF 10% 50V 0603 | TDK | C1608JB1H331 KT000N | CAP0603 |
| 16 | 2 | C137-138 | CAP CER 33pF 10% | AVX CORP | 0603YC330JAT 2A | CAP0603 |

| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|--------|-----|---|---|----------------------|------------------------|---|
| | | | 16V NPO 0603 | | | |
| 17 | 14 | C13 C17 C20 C94 C114 C120 C128 C135 C139 C141 C146 C161 C166-167 | CAP CER 4.7uF 10% 10V X5R 0603 | TDK | C1608X5R1A47 5K | CAP0603 |
| 18 | 2 | C74 C162 | CAP CER 4.7uF 10% 35V X5R 0603 | MURATA | GRM188R6YA4 75KE15D | CAP0603 |
| 19 | 2 | C48 C173 | CAP CER 4.7uF 10% 25V 0805 | MURATA | GRM21BR61E4 75KA12L | CAP0805 |
| 20 | 12 | C45-47 C54-56 C80-82 C168-170 | CAP CER 4.7uF 10% 50V X7R 0805 | MURATA | GRM32ER71H4 75KA88L | CAP0805 |
| 21 | 1 | C147 | CAP CER 10uF 10% 6.3V X5R 1206 | SAMSUNG | CL31A106KQH NNNE | CAP1206 |
| 22 | 1 | C148 | CAP ELECT 100uF 20% 10V FK SMD | UNITED CHEMI- CON | EMVA100ADA1 01MF55G | CAPELEC_ ALUM_6.3 MM DIA |
| 23 | 1 | C110 | CAP ELECT 10uF 20% 50V FK SMD | PANASONIC | EEV- FK1H100UR | CAPELEC_ ALUM_5X5 .8MM_FK_ SMD |
| 24 | 1 | C143 | CAP ELECT 10uF 20% | PANASONIC | ECEA1HKS100 | TH |

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| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|--------|-----|-----------------------------------|---|--------------------------|----------------------|-------------------|
| | | | 50V TH RADIAL | | | |
| 25 | 3 | CT1-3 | CAP 22uF TANT 6.3V 10% case size-c/6032- 28 SMD | KEMET | T495C226 | CAPTANT_ T491C |
| 26 | 4 | CL1-4 | COMMON MODE FILTER SMD | BOURNS | SRF0905-500Y | SMD |
| 27 | 1 | CON1 | TER BLOCK 2POS. 2.54MM PCB | ON SHORE TECH | OSTVN02A150 | TH 2.54MM |
| 28 | 8 | J1-4 J6-9 | CONN.TERM BLOCK 2POS. 5MM PCB | PHONIX CONTACT | 1935161 | TH_5MM |
| 29 | 1 | J5 | J-TAG CONNECTE R 14-PIN | TE CONN. | 1-1634688-4 | 14-PIN J- TAG |
| 30 | 1 | Y1 | CRYSTAL 10MHZ 18PF 60 OHM | CTS FREQUENCY CONTROL | ATS100B-E | TH HOLE |
| 31 | 5 | R31 R56 R74 R130 R132 | RES 2.2 Ohm 1% 1/10W 0603 | YAGEO | RC0603JR- 072R2L | RES0603 |
| 32 | 10 | R5-9 R13 R110 R113 R118-119 | RES 1k 1% 1/10W 0603 | Vishay/Dale | CRCW06031K0 0FKEA | RES0603 |
| 33 | 1 | R82 | RES 7.5k 1% 1/10W 0603 | Vishay/Dale | ERJ- 3EKF1202V | RES0603 |

| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
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| 34 | 3 | R12 R91 R127 | RES 0.0 OHM 5% 1/10W 0603 | VISHAY/DALE | CRCW0603000 0Z0EB\ | RES0603 |
| 35 | 1 | D5 | DIODE MBAT46W-V 100V 150MA SOD123 | VISHAY SEMI. | BAT46W-E3- GSO8 | SOD123 |
| 36 | 1 | D13 | DIODE ZENER 2.2V 500MW SOD-123 | ON Semiconductor | MMSZ4680TIG | SOD-123 |
| 37 | 3 | D1-3 | DIODE ZENER DNP SOD-123 | | DNP | SOD-123 |
| 38 | 5 | CON2-6 | CON 12POS 2.54 pitch DUAL T- HOLE | SULLINS CONN. | EBC06MMMD | CON2X6 |
| 39 | 2 | U7 U19 | IC PRECISION REF 1.5VREF SOT23 | INTERSIL | ISL21010CFH3 15Z | SOT23-3 |
| 40 | 1 | U10 | IC CURRENT SENSOR | LINEAR TECH. | LT3092EST#PB F | SOT223-3 |
| 41 | 1 | U11 | IC DIGITAL ISO 3CH TRI- STATE 16SOIC | SI8430 | SI8430AB-D-IS1 | SOIC16 |
| 42 | 8 | D4 D6-12 | LED RED 0805 SMD | ROHM | SML-211UTT- 86 | LED0805 |

| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|--------|-----|-------------|--|-------------------------|-------------------|----------|
| 43 | 1 | U23 | IC LF50ABDT REG 1.5A 5VOLT DPAK | STMicroelectronics | LF50ABDT | DPAK |
| 44 | 1 | U12 | IC LM258 Dual OpAmp SOIC8 | ST MICRO | LM258DT | SOIC8 |
| 45 | 1 | U1 | microcontroller TMS320F28377D | TEXAS INSTRUMENT | TMS320F28377DPTPT | LQFP-176 |
| 46 | 3 | U13 U15 U21 | IC BUFFER NONINVERTING SOIC14 | FAIRCHILD SEMICONDUCTOR | MC74VHCT50A | SOIC14 |
| 47 | 3 | U3 U5 U9 | IC MCP6031 single OpAmp SOIC8 | Microchip | MCP6031-E/SN | SOIC8 |
| 48 | 8 | Q2-9 | TRANS MMBT2222A GP NPN SOT23 | FAIRCHILD | MMBT2222A | SOT23 |
| 49 | 2 | U16-17 | OPTICAL SWITCH, TRANSISTOR OUTPUT 4SMD | SHARP MICRO ELECTRIC | PC817XNNIP0F | 4SMD |
| 50 | 1 | U20 | TVS DIODE 5.5VWM 8VC 8MSOP | ST MICRO | PACDN046MR | 8MSOP |
| 51 | 1 | VR1 | POT 1K OHM 1/4W PLASTIC LINEAR | BOURNS | 3310Y-001-102L | TH |

| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
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| 52 | 4 | PS1-4 | 0.25W, FIXED INPUT, ISOLATED & UNREGULA TED SINGLE OUTPUT | MORNSON | B0505XT-1WR2 | SMD |
| 53 | 1 | U18 | IC REF3230 SERIES VOLTAGE REFERENCE | TEXAS | REF3230AIDBV T | SOT23-6 |
| 54 | 9 | R79 R84 R92 R100 R103 R108-109 R116-117 | RES 0.0 OHM 1/10W 5% 0603 | VISHAY/DALE | CRCW0603000 0Z0EA | RES0603 |
| 55 | 1 | R104 | RES 1.5k 1% 1/10W 0603 | Vishay/Dale | CRCW06031K5 0FKEA | RES0603 |
| 56 | 7 | R1-2 R59 R61 R107 R114 R129 | RES, 100K, 1%. 1/10W, 0603, TF | Vishay/Dale | CRCW0603100 KFKEA | RES0603 |
| 57 | 3 | R3 R10 R142 | RES 100 Ohm 1% 1/10W 0603 | Vishay/Dale | CRCW0603100 RFKEA | RES0603 |
| 58 | 7 | R11 R46 R51 R60 R98 R134 R4 | RES 100 Ohm 1% 1/10W 0603 | Vishay/Dale | CRCW0603100 RFKEA | RES0603 |
| 59 | 2 | R52-53 | RES 10.0 OHM 0.1% 1/10W 0603 | Vishay/Dale | TNPW060310R 0BEEA | RES_0603 |
| 60 | 29 | R14-15 R19- 22 R26-29 R38-41 R75- 78 R80-81 | RES, 10K, 1%. 1/10W, 0603, TF | Vishay/Dale | CRCW060310K 0FKEA | RES0603 |

CPWR-AN24, Rev -, 06-2018

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| | | R120-125 R128 R135-136 | | | | |
| 61 | 5 | R63 R65 R73 R88-89 | RES, 1K, 1%. 1/10W, 0603, TF | Vishay/Dale | CRCW06031K0 0FKEA | RES0603 |
| 62 | 1 | R17 | RES 1M 1% 1/10W 0603 | VISHAY/DALE | CRCW06031M0 0FKEA | RES0603 |
| 63 | 3 | R93 R101-102 | RES, 2.2K, 1%. 1/10W, 0603, TF | Vishay/Dale | CRCW060310K 0FKEA | RES0603 |
| 64 | 6 | R105-106 R111-112 R138 R140 | RES 22K 1% 1/10W 0603 | PANASONIC-ECG | ERJ- 3EKF2202V | RES0603 |
| 65 | 2 | R57-58 | RES, 27K, 1%. 1/10W, 0603 | VISHAY | CRCW060327K 0FKEA | RES0603 |
| 66 | 1 | R45 | RES 2K 1% 1/10W 0603 | VISHAY/DALE | ERJ- 3EKF1202V | RES0603 |
| 67 | 1 | R131 | RES 2K 1% 1/10W 0603 | VISHAY/DALE | ERJ- 3EKF1202V | RES0603 |
| 68 | 8 | R83 R94-97 R99 R137 R139 | RES 3.3K 1% 1/10W 0603 | VISHAY/DALE | CRCW06033K3 0FKEA | RES0603 |
| 69 | 10 | R32-36 R42-44 R68 R115 | RES 4.7E 1% 1/10W 0603 | YAGEO | RC0603JR- 074R7L | RES0603 |
| 70 | 5 | R30 R55 R72 R126 R133 | RES 4.7 K 1% 1/10W 0603 | VISHAY/DALE | MC00063W060 314K7 | RES0603 |
| 71 | 1 | R54 | RES 470K 1% 1/10W 0603 | PANASONIC | ERJ- 3EKF4703V | RES0603 |

| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|--------|-----|----------------------------|----------------------------------|--------------|----------------------|---------|
| 72 | 1 | R49 | RES 470 OHM 1% 1/10W 0603 | Vishay/Dale | CRCW0603470 RFKEA | RES0603 |
| 73 | 1 | R90 | RES 470 OHM 1% 1/10W 0603 | Vishay/Dale | CRCW0603470 RFKEA | RES0603 |
| 74 | 1 | R48 | RES 47K 1% 1/10W 0603 | VISHAY/DALE | CRCW060347K 0FKEA | RES0603 |
| 75 | 1 | R16 | RES, 5.1K, 1%. 1/10W, 0603 | PANASONIC | ERJ- 3EKF5101V | RES0603 |
| 76 | 1 | R18 | RES 6.26K 1% 1/10W 0603 | PANASONIC | ERJ- 3EKF60261V | RES0603 |
| 77 | 1 | R143 | RES0603 6.8K 5% 1/10W | PANASONIC | ERJ- 3GEYJ682V | RES0603 |
| 78 | 1 | R37 | RES 7.8K 1% 1/10W 0603 | VISHAY/DALE | CRCW06037K8 FKEA | RES0603 |
| 79 | 1 | R50 | DNP | | DNP | RES0603 |
| 80 | 1 | R47 | RES DNP 1% 1/10W 0603 | Vishay/Dale | DNP | RES0603 |
| 81 | 4 | R147-150 | RES2512 10 OHM 5% 1W | PANASONIC | ERJ-1TYJ100U | RES1206 |
| 82 | 2 | R62 R87 | RES1206 1K 1% 1/4W | PANASONIC | P1.0KECT | RES1206 |
| 83 | 4 | R64 R66-67 R151 | RES 220K 1% 1/4W 1206 | VISHAY/DALE | CRCW12061M0 0FKEA | RES1206 |
| 84 | 9 | R23-25 R69- 71 R144-146 | RES1206 470K 1%1/4W | PANASONIC | ERJ- 8ENF4703V | RES1206 |

| Sr. No | Qty | Reference | Description | Manufacturer | Manufacturer P/N | PACKAGE |
|--------|-----|-----------|-------------------------------------|---------------------|-----------------------|----------------|
| 85 | 1 | R141 | RES 15 Ohms 1% 1/4W 1210 | PANASONIC | ERJ-14YJ150V | RES1210 |
| 86 | 2 | R85-86 | RES 20 Ohms 1% 1/4W 1210 | PANASONIC | ERJ-14YJ200V | RES1210 |
| 87 | 1 | SW1 | SWITCH SLIDE SPDT 300MA 6V | E-SWITCH | EG1270 | TH_2.54M M |
| 88 | 1 | SW2 | SWITCH TOGGLE SPDT 0.4VA | NKK SERIES | B12AB | SWT_TH SPDT |
| 89 | 1 | U22 | IC REG LDO 3.3V/1.2V 24HTSSOP | TEXAS INSTRUMENT | TPS70445PWP | TSSOP24 |
| 90 | 2 | U6 U14 | VAC CURRENT SENSOR | VAC | T60404-N4646- X161 | TH_4PIN |

7. References

- [1] Robert L Steilgerwald, "A Comparison of Half-Bridge Resonant Converter Topologies", IEEE Transactions on Power Electronics, Vol.3, No.2, April 1988.
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- [3] C. C. Chan and K. T. Chau, "An overview of power electronics in electric vehicles," *Industrial Electronics, IEEE Transactions on*, vol. 44, pp. 3-13, 1997.
- [4] J. Tianyang, Z. Junming, W. Xinke, S. Kuang, and W. Yousheng, "A Bidirectional LLC Resonant Converter With Automatic Forward and Backward Mode Transition," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 757-770, 2015.
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- [7] B. Yang, "Topology investigation for front end DC/DC power conversion for distributed power system," Virginia Polytechnic Institute and State University, 2003.
- [8] W. Kramer, S. Chakraborty, B. Kroposki, A. Hoke, G. Martin, and T. Markel, "Grid Interconnection and Performance Testing Procedures for Vehicle-To-Grid (V2G) Power Electronics," National Renewable Energy Laboratory (NREL), Golden, CO. 2012.

8. Revision History

| Date | Revision | Changes |
|-----------|----------|-------------|
| June 2018 | | First issue |

IMPORTANT NOTES

Purposes and Use

Cree, Inc. (on behalf of itself and its affiliates, “Cree”) reserves the right in its sole discretion to make corrections, enhancements, improvements, or other changes to the board or to discontinue the board.

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It is important to operate the board within Cree’s recommended specifications and environmental considerations as described in the Documentation. Exceeding specified ratings (such as input and output voltage, current, power, or environmental ranges) may cause property damage. If you have questions about these ratings, please contact Cree at sic_power@cree.com prior to connecting interface electronics (including input power and intended loads). Any loads applied outside of a specified output range may result in adverse consequences, including unintended or inaccurate evaluations or possible permanent damage to the board or its interfaced electronics. Please consult the Documentation prior to connecting any load to the board. If you have any questions about load specifications for the board, please contact Cree at sic_power@cree.com for assistance.

Users should ensure that appropriate safety procedures are followed when working with the board as serious injury, including death by electrocution or serious injury by electrical shock or electrical burns can occur if you do not follow proper safety precautions. It is not necessary in proper operation for the user to touch the board while it is energized. When devices are being attached to the board for testing, the board must be disconnected from the electrical source and any bulk capacitors must be fully discharged. When the board is connected to an electrical source

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and for a short time thereafter until board components are fully discharged, some board components will be electrically charged and/or have temperatures greater than 50° Celsius. These components may include bulk capacitors, connectors, linear regulators, switching transistors, heatsinks, resistors and SiC diodes that can be identified using board schematic. Users should contact Cree at sic_power@cree.com for assistance if a board schematic is not included in the Documentation or if users have questions about a board's components. When operating the board, users should be aware that these components will be hot and could electrocute or electrically shock the user. As with all electronic evaluation tools, only qualified personnel knowledgeable in handling electronic performance evaluation, measurement, and diagnostic tools should use the board.

User Responsibility for Safe Handling and Compliance with Laws

Users should read the Documentation and, specifically, the various hazard descriptions and warnings contained in the Documentation, prior to handling the board. The Documentation contains important safety information about voltages and temperatures.

Users assume all responsibility and liability for the proper and safe handling of the board. Users are responsible for complying with all safety laws, rules, and regulations related to the use of the board. Users are responsible for (1) establishing protections and safeguards to ensure that a user's use of the board will not result in any property damage, injury, or death, even if the board should fail to perform as described, intended, or expected, and (2) ensuring the safety of any activities to be conducted by the user or the user's employees, affiliates, contractors, representatives, agents, or designees in the use of the board. User questions regarding the safe usage of the board should be directed to Cree at sic_power@cree.com.

In addition, users are responsible for:

- compliance with all international, national, state, and local laws, rules, and regulations that apply to the handling or use of the board by a user or the user's employees, affiliates, contractors, representatives, agents, or designees.
- taking necessary measures, at the user's expense, to correct radio interference if operation of the board causes interference with radio communications. The board may generate, use, and/or radiate radio frequency energy, but it has not been tested for compliance within the limits of computing devices pursuant to Federal Communications Commission or Industry Canada rules, which are designed to provide protection against radio frequency interference.

- compliance with applicable regulatory or safety compliance or certification standards that may normally be associated with other products, such as those established by EU Directive 2011/65/EU of the European Parliament and of the Council on 8 June 2011 about the Restriction of Use of Hazardous Substances (or the RoHS 2 Directive) and EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (or WEEE). The board is not a finished product and therefore may not meet such standards. Users are also responsible for properly disposing of a board's components and materials.

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