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Industrial and Body Diode Qualification of Gen-III Medium Voltage SiC MOSFETs: Challenges and Solutions

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Abstract. In this work, we report the results of industrial qualification tests run on medium voltage SiC MOSFETs rated for 3.3 kV/40 A and 10 kV/15 A. The JEDEC JESD47J.01 standard was used as a guideline to conduct HTRB (High Temperature, Reverse Bias), HTGB (High Temperature, Gate Bias), and TDDB (Time Dependent Dielectric Breakdown) tests. No devices were found to have failed the qualification tests, and long oxide lifetime was projected for constant operation under positive bias. This paper also reports for the first time the results of qualification testing of the MOSFET body diode on a large population of medium voltage SiC MOSFETs. Constant current stress at a current equal to the device forward rating was applied for 1000 hours. No degradation of any device parameter was observed for 3 lots of devices at both the 3.3 kV and 10 kV voltage rating.

Introduction

Medium voltage unipolar 4H-SiC power devices have captured the imaginations of power device and circuit designers for as long as quality 4H-SiC material has been available. 4H-SiC power MOSFETs with blocking voltages of 10 kV were demonstrated nearly 7 years prior to the commercial introduction of 1200 V MOSFETs [1]. There has been strong interest in the utilization of medium voltage 4H-SiC devices for grid-tied inverters [2], traction power conversion and distribution [3], and wind power conversion [4].

Nonetheless, there are only limited commercial offerings of 4H-SiC 3.3 kV MOSFETs [3], and no qualified MOSFET products that are available at higher voltage ratings. The lack of qualified parts leads to assumptions of general unreliability of 4H-SiC in medium voltage applications [5]. In addition, recombination-enhanced stacking fault glide at basal plane dislocations [6] presents a fundamental material challenge for reliable 4H-SiC bipolar device operation. Previous studies have reported stable medium voltage bipolar devices in silicon carbide [7], although quantities were limited to four devices in that study. In addition, there have been large, high current 3.3 kV modules available on the market since 2015 [3], indicating a high degree of technological maturity, although bipolar stability still appears to be a topic of discussion [8].

This work presents the results of qualification testing of the Wolfspeed Gen-III 3.3 kV and 10 kV medium voltage MOSFETs. The technological maturity of Wolfspeed SiC Medium Voltage MOSFETs has advanced to the point where none of the standard industrial qualification tests present an insurmountable challenge, however, the act of conducting the qualification tests themselves is nontrivial, and care must be taken to ensure the tests provide good data fidelity.

Gen-III Medium Voltage MOSFET Device Structure

A detailed description of Wolfspeed Gen-III medium voltage MOSFET development was first reported in [9] and [10], along with all relevant device parameters. Subsequent optimization of device layouts to maximize active area as well as optimize the internal gate resistance for good trade-off between switching speed and ease of integration has led to the device top layouts shown in Fig. 1. The basic drift structure has remained unchanged since the first reports (27 µm/2.8e15 cm^{-3} drift for the 3.3 kV MOSFET, and 100 µm/6e14 cm^{-3} drift for the 10 kV MOSFET); the choice of drift doping and thickness is constrained by the optimal 1D limit, and achieved device resistances are not far from ideal predictions [10]. The device edge termination design has also remained unchanged since reported in [9], and consists of field limiting guard rings. The chip layout of the 3.3 kV MOSFET has changed since initial reports for optimal integration into the Wolfspeed XHV-7 power module, with a slightly smaller chip area (38 mm^2 vs. 43 mm^2). This smaller chip area allows for one additional chip per switch position to be used for an overall increase in module current. The 10 kV MOSFET total area has remained unchanged since initially reported in [10], however, a reduction in gate runners has allowed for an increase of the active area per chip from 29 mm^2 to 31 mm^2 at the cost of a slightly increased internal gate resistance. In addition, the gate oxide has been thickened in the 10 kV MOSFET to lower gate drive fields, increasing current saturation for additional short-circuit withstand time. At the time of testing, the approximate current rating of the 3.3 kV devices was 40 A at 175 °C, and the 10 kV device was 15 A at 175 °C.

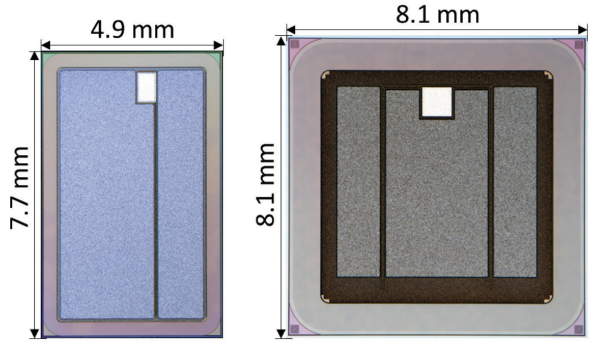

Fig. 1. Die photographs of Gen-III 3.3 kV/40 A MOSFET (left) and 10 kV/15 A MOSFET (right).

Industrial Qualification of SiC Medium Voltage MOSFET Gate Oxide

Challenges in Qualification of Medium Voltage MOSFET gate. The MOSFET gate structure is primarily tested in the HTGB test, which involves grounding the source and drain terminals of the MOSFET, and applying a positive or negative bias to the gate to induce an electric field in the gate dielectric that is equal to the field under maximum operating voltage and temperature. This is illustrated in Fig. 2. In addition to the HTGB test, ESD testing was also performed, which is a test of dielectric strength of the MOSFET gate oxide as well as immunity of the device to extreme dv/dt transients. For Silicon Carbide MOSFETs, the roughness of the epitaxial surface is of concern, as threading dislocations can introduce pits into the surface that have depths on the order of the thickness of the gate oxide [11]. In addition to the features introduced by threading dislocations, in the case of a 10 kV epitaxial layer, even the RMS roughness of the surface is approximately 14 nm [12]. Once these manufacturing challenges are overcome, the qualification test is relatively easy to carry out. For the HTGB test, standard TO-247 packaging was used to carry the 3.3 kV and 10 kV MOSFETs. Although this does not allow for testing of the drain blocking performance, this structure is not stressed during the HTGB test and due to the sensitivity of the gate leakage measurement to device failure, this provides a relevant evaluation of device performance. For the ESD testing, high voltage test packages were used to ensure no damage was induced in the edge termination region.

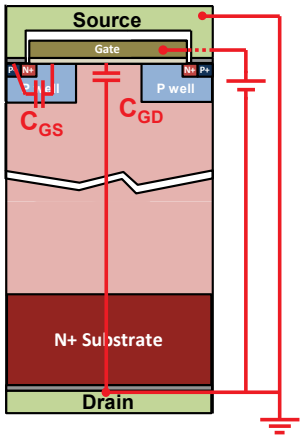

Fig. 2. Schematic diagram of stressed MOSFET structures in HTGB and ESD tests.

HTGB and ESD qualification results. The *in-situ* monitored gate current traces for 75x 3.3 kV MOSFETs (25 devices from each of 3 fabrication lots) and the same quantity of 10 kV MOSFETs are shown in Fig. 3. (a) and Fig. 3. (b) respectively. The gate voltage used was 15 V, and the temperature during test was 175 °C. No device failures were observed in the test. The testing was repeated at gate voltage of 19 V for 1000 more hours, which also resulted in no failures.

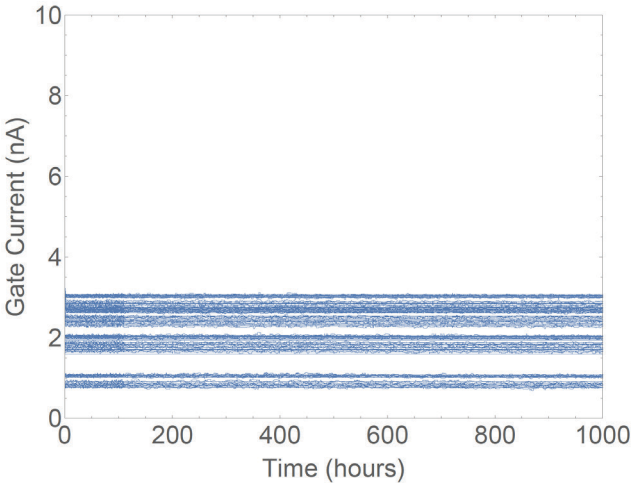

Fig. 3. (a) *In-situ* monitored gate current during HTGB test of 3x25 3.3 kV, 40 A MOSFETs.

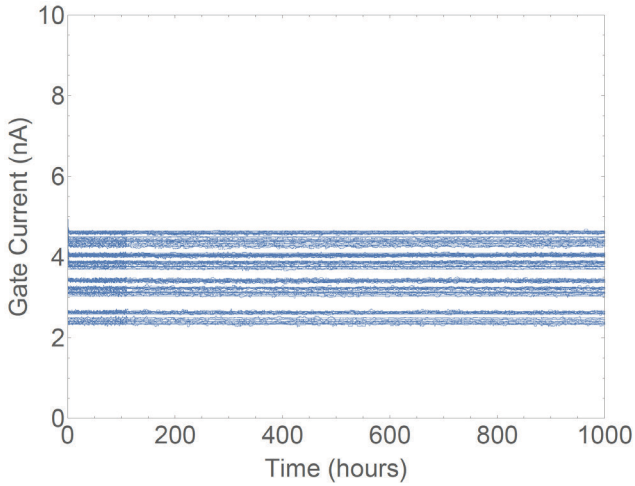

Fig. 3. (b) *In-situ* monitored gate current during HTGB test of 3x25 10 kV, 15 A MOSFETs.

ESD testing was carried out using dedicated test equipment to qualify the devices to the 8 kV (Class 3B) HBM (Human Body Model) level, and the 1 kV (Class IV) CDM (Charged Device Model) level. No degradation in either gate or drain leakage was observed after ESD testing.

TDDB life projections. To project intrinsic life, TDDB was performed on a population of 30 parts per voltage class at 175 °C at 3 different voltage stress levels per voltage class to extract a field acceleration factor and thus project useful life. The life projections for the 3.3 kV and 10 kV MOSFETs are shown in Fig. 4. (a) and (b) respectively. Longer life is projected for the 10 kV MOSFET due to the use of a thicker gate oxide as mentioned in the previous section.

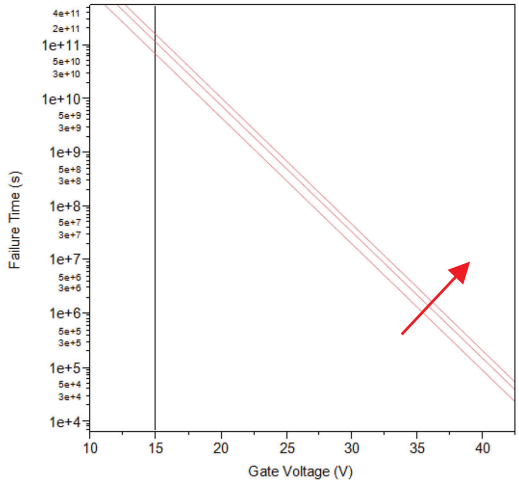

Fig 4. (a) Intrinsic gate lifetime projection for 3.3 kV MOSFETs at 175 °C.

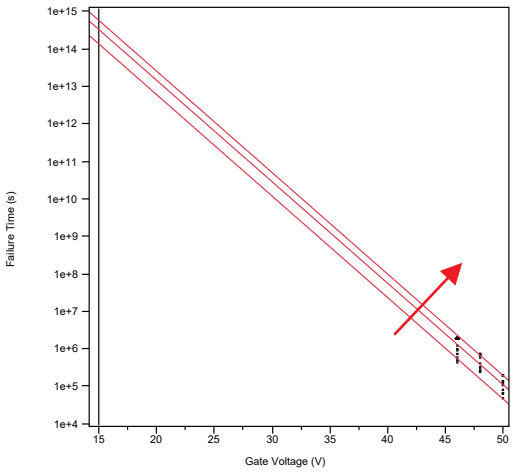

Fig 4. (b) Intrinsic gate lifetime projection for 10 kV MOSFETs at 175 °C.

Blocking Structure Qualification through HTRB test

Challenges in Qualification and Testing of Medium Voltage SiC MOSFETs in the Blocking Mode. The HTRB test is designed to determine if there are any weaknesses in a MOSFET structure under long term stress with high voltage applied to the drain terminal and in high ambient temperature. The device structures stressed are shown in Fig. 5. For the 3.3 kV class tests, which are carried at 2640 V drain bias and 175 °C, the relevant voltage stress is largely confined to the semiconductor device and package. However, for the 10 kV device HTRB test, which was carried out at 8 kV, a significant amount of voltage stress is applied to the HTRB oven and test boards. During testing, partial discharge can destroy test sockets, resulting in false failures. Care must be taken to ensure adequate separation of ground and bias planes, as well as to eliminate any sources of corona discharge. Test system issues were discovered and eliminated during the HTRB qualification of the 10 kV, 15 A 4H-SiC Schottky diode, allowing the MOSFET HTRB qualification to proceed without interruption.

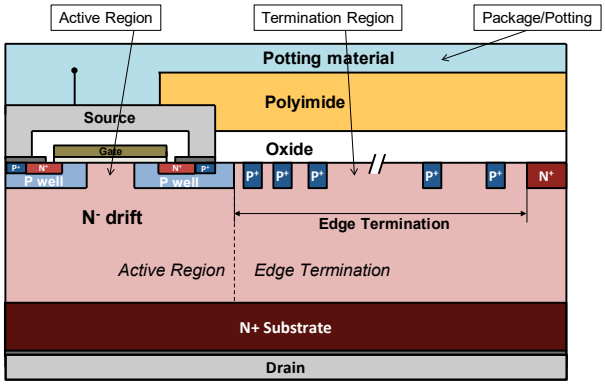

Fig. 5. Schematic diagram of stressed MOSFET structures in HTRB test.

Medium Voltage MOSFET HTRB Qualification Results. The *in-situ* monitored drain current traces for 75x 3.3kV MOSFETs (25 devices from each of 3 fabrication lots) and the same quantity of 10 kV MOSFETs are shown in Fig. 6. (a) and Fig. 6. (b) respectively. No failures were observed *in-situ* or upon measurement at room temperature, although some leakage spikes were observed in the 10 kV MOSFET *in-situ* monitored traces. The cause of these current spikes is unknown, but based on the lack of failures during the post-stress electrical measurement and the spike's rapid disappearance after initiation, they are believed to be an internal short within the test system that self-healed after initiation.

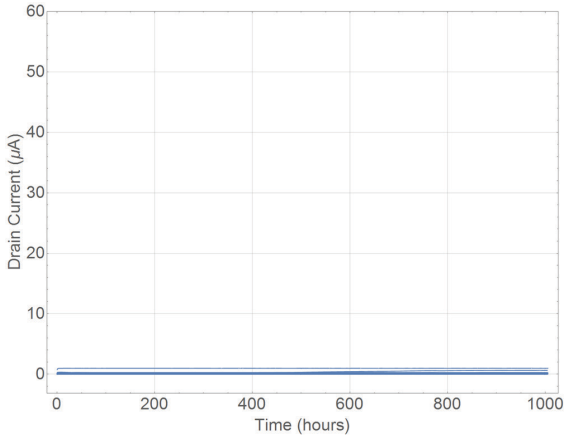

Fig. 6. (a) *In-situ* monitored drain current during HTRB test of 3x25 3.3 kV, 40 A MOSFETs at 2640 V drain bias and 175 °C.

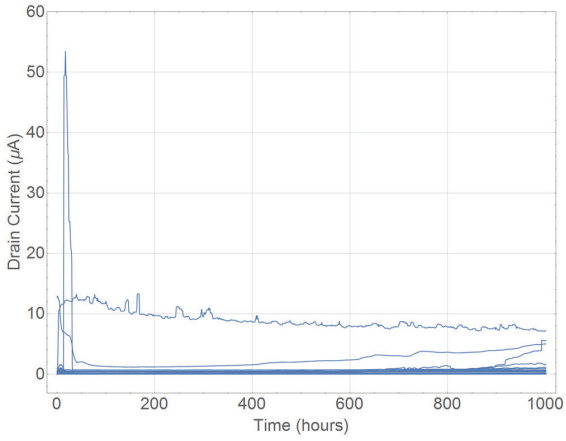

Fig. 6. (b) *In-situ* monitored drain current during HTRB test of 3x25 10 kV, 15 A MOSFETs at 8 kV drain bias and 175 °C.

Accelerated life testing was not conducted to project useful life at high drain bias, however, as the failure mode is expected to be dielectric breakdown within the MOSFET JFET gap [13], the lifetime can be expected to be as good or better than Wolfspeed Gen-II 1200 V parts, which already have extremely long projected lifetimes [14]. The reason for this is thicker drift regions in higher voltage MOSFETs have a lower electric field in the blocking mode than thinner ones in lower

voltage MOSFETs, as defined by the solution to the ionization integral [15]. Thus, significantly longer lifetimes can be expected of medium voltage 4H-SiC MOSFETs when compared to their lower voltage counterparts, given the same cell structure.

MOSFET Body Diode Qualification

Challenges in Qualification of Medium Voltage MOSFET Body Diode. The topic of bipolar degradation in 4H-SiC has a long history; the reader is encouraged to find other sources for more detail on this topic. Modern Wolfspeed 4H-SiC substrate production practices have resulted in a massive decrease in the basal plane dislocation content when compared to that reported in initial studies [16], and thus provide a template for growth of sufficiently low BPD epitaxy to allow for production of medium voltage MOSFETs.

With regards to conducting a qualification test, constant current stressing was chosen for the reason that it leads to a minimum time-to-results and is easier to integrate than a pulsed solution. For the currents and voltages of consideration (40 A with approximately 6 V of drop in the case of the 3.3 kV MOSFET, and 15 A with approximately 9 V of drop in the case of the 10 kV MOSFET), it is possible to obtain COTS (component-off-the-shelf) constant current power supplies that will perform the required function. Dissipating the 240 W of thermal power then becomes the primary challenge, which was accomplished by use of forced-air cooled individual heatsinks. The junction temperature was allowed to equilibrate at a point determined by the heatsink cooling capacity and input power. This resulted in a T_J of approximately 70 °C for the 10 kV MOSFET, and approximately 140 °C for the 3.3 kV MOSFET. -5 V was applied between the gate and the source terminals of the devices under test to eliminate all channel current.

Medium Voltage MOSFET Body Diode Qualification Results. The *in-situ* monitored body diode source voltage traces are shown in Fig. 7. (a) and (b) for the 3.3 kV, 40 A MOSFET and 10 kV, 15 A MOSFET, respectively. Sixty-five (65) 10 kV MOSFETs were tested, and sixty-one (61) 3.3 kV MOSFETs were tested, representing 3 distinct fabrication lots. No significant increase in body diode forward voltage was observed for any tested device, indicating that Wolfspeed medium voltage MOSFET structure achieves bipolar stability in the 3rd quadrant.

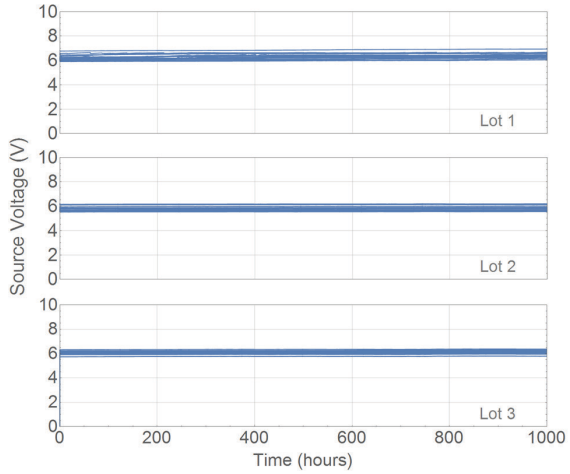

Fig. 7. (a) *In-situ* monitored source voltage during BDOL (body diode operating life) test of 3.3 kV, 40 A MOSFETs at I_{SD}=40 A.

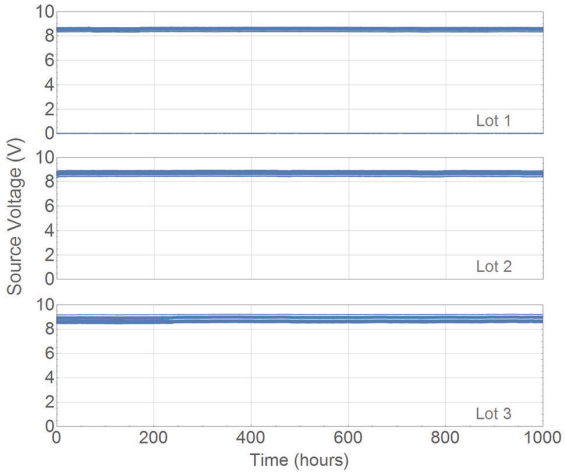

Fig. 7. (b) *In-situ* monitored source voltage during BDOL test of 10 kV, 15 A MOSFETs at I_{SD}=15 A.

Reference [17] reported an increase in unipolar resistance following bipolar stress of medium voltage 4H-SiC diodes. This parameter was also examined by comparing MOSFET on-resistance before and after stress, which is plotted as distributions in Fig. 8. The on-resistance shift percentages were found to be less than 10 % in all cases, and indeed, a significant fraction of devices were found to have decreased in on-resistance. This was attributed to the lack of a die kelvin sense terminal

leading to significant test-to-test measurement variation. In addition, no shifts were observed in drain leakage or threshold voltage.

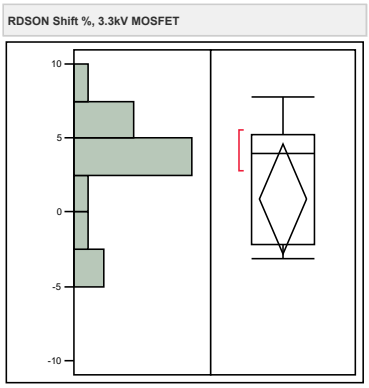

Fig. 8. (a) On-resistance shift between pre-BDOL and post-BDOL measurement for 3.3 kV MOSFETs.

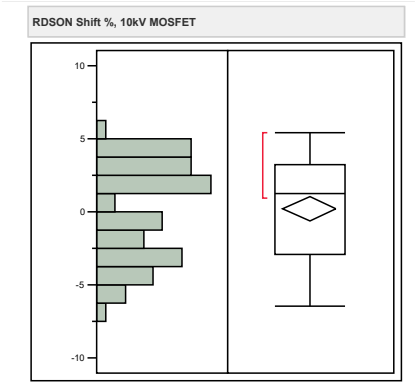

Fig. 8. (b) On-resistance shift between pre-BDOL and post-BDOL measurement for 10 kV MOSFETs.

Discussion and Perspective

The successful qualification testing performed on Wolfspeed medium voltage MOSFETs is an important step towards full commercial release and fulfillment of the initial promise of 4H-SiC power devices. With high quality, reliable, and rugged medium voltage MOSFETs offered from Wolfspeed as well as other manufacturers, we now move into an era where the 4H-SiC material system is accepted as state-of-art in the semiconductor industry.

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