CPWR-AN46:

CGD1700HB2M-UNA Dual Channel Differential Isolated Half-Bridge Gate Driver Board User Guide

CGD1700HB2M-UNA
DUAL CHANNEL DIFFERENTIAL ISOLATED HALF-BRIDGE GATE DRIVER BOARD USER GUIDE

Note: *Cree prepared various documents, which may include a User's Guide or an Application Note, that describe the proper operation and safe usage of the various evaluation boards to which this half-bridge board may be attached. Please review any documents that describe the use of the applicable evaluation boards that are located at http://wolfspeed.com/power/products/reference-designs (in the case of reference designs) or the appropriate product page at https://www.wolfspeed.com/power/products/gate-driver-boards (in the case of boards) for information and warning statements about the proper usage of the evaluation boards. YOU MUST READ ALL OF THE DOCUMENTS THAT APPLY TO THE APPLICABLE EVALUATION BOARDS AND ARE DESCRIBED IN THIS PARAGRAPH BEFORE YOU OPERATE THE EVALUATION BOARDS. DEATH OR SERIOUS INJURY, INCLUDING ELECTROCUTION, ELECTRICAL SHOCK, OR SEVERE BURNS, CAN OCCUR IF AN EVALUATION BOARD IS IMPROPERLY USED OR IF PROPER SAFETY PRECAUTIONS ARE NOT FOLLOWED.*

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1. Product Scope

CGD1700HB2M-UNA is a half bridge gate driver board for evaluation of Wolfspeed® C3M™ SiC MOSFETs and modules. This board is intended to be used in conjunction with Wolfspeed evaluation boards.

2. Features

- Optimized for Wolfspeed high- performance C3M SiC MOSFETs and modules
- Texas Instruments® (TI) UCC21710 ±10-A, 5.7-kV RMS single channel isolated gate driver with overcurrent protection
- On-Board 2W isolated power supplies
- DC supply reverse polarity protection
- Differential inputs for increased noise immunity
- Single-ended to differential daughter board (CGD12HB00D) sold separately

Please see "Important Notes" below regarding the supply of this board by Cree.

3. Maximum Ratings

Symbol	Parameter	Value	Unit
$V_{DC\ BUS}$	Max DC Bus Voltage	1400	V
V_{IN}	Supply Voltage	-0.5 - 13.2	V
V_I	Logic Level Input pins LS-PWM-N, LS-PWM-P, HS-PWM-N, HS-PWM-P, Reset Input	-0.5 to 7	V
V_O	Logic Level Output pins RTD-Output-P, RTD-Output-N, FAULT-Output-P, FAULT-Output-N	-0.5 to 7	V
Fs	Maximum switching frequency (limited by gate power supply)	1	MHz
T_{op}	Ambient Operating Temperature	-50 to 70	°C
T_{stg}	Storage Temperature	-50 to 125	

4. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IN}	Supply Voltage	10.8	12	13.2	V	
Single Ended Input (SN65C1167EPWR)						
V_{IH}	High Level Logic Input Voltage	2.0				Single-Ended Inputs
V_{IL}	Low Level Logic Input Voltage			0.8		
Differential Inputs (SN65C1167EPWR)						
V_{IDCM}	Differential Input Common Mode Range	-7		+7		
V_{IDTH}	Differential Input Threshold Voltage	-200		+200	mV	$V_{ID}=V_{Pos\text{-}Line} - V_{Neg\text{-}Line}$

V_{HYST}	Differential Voltage Hysteresis		60			
V_{ODH}	Differential Output High Level	2.4	3.5		V	I_{OD} = -20 mA
V_{ODL}	Differential Output Low Level		0.2	0.4		I_{OD} = 20 mA
V_{OD}	Differential Output Magnitude	2	3.7			R_L=100 Ω
$t_{PHL/PLH}$	Propagation Delay		8		ns	C_L = 30 pF

5. Gate Driver Block Diagram

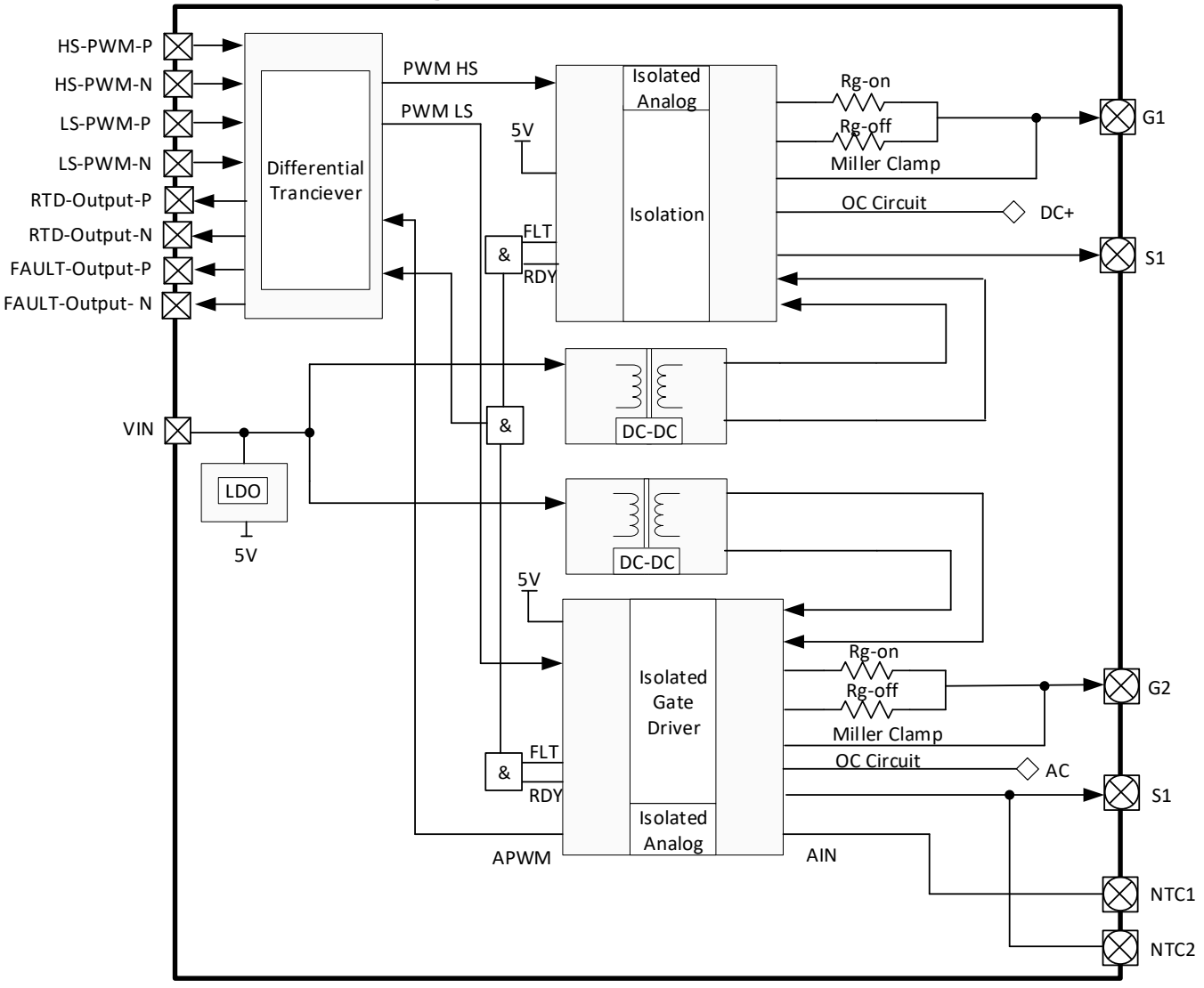

Figure 1. Gate Driver Block Diagram

6. Input / Output Connector Information

Pin Number	Name	Description
1	VIN	12V Power Supply Input Pin
2	Common	Common
3	HS-PWM-P*	High Side PWM Signal – Positive Differential, Active High
4	HS-PWM-N*	High Side PWM Signal – Negative Differential, Active Low
5	LS-PWM-P*	Low Side PWM Signal – Positive Differential, Active High.
6	LS-PWM-N*	Low Side PWM Signal – Negative Differential, Active Low.
7	/FAULT-Output-P*	Fault Output – Positive Differential, Active Low **Caution for 3.3 V systems: this output is 5 V**
8	/FAULT-Output-N*	Fault Output – Negative Differential Active High **Caution for 3.3 V systems: this output is 5 V**
9	RTD-Output-P*	5 V Temperature Dependent Resistor Output – Positive Differential **Caution for 3.3 V systems: this output is 5 V.** Duty cycle modulated.
10	RTD-Output-N*	5 V Temperature Dependent Resistor Output – Negative Differential **Caution for 3.3 V systems: this output is 5 V.** Duty cycle modulated.
11	NC	No Connect
12	Common	Common
13	NC	No Connect
14	Common	Common
15	Reset Input	Buffered and passed through to gate driver. Refer to the gate driver datasheet available from TI for RST/EN functionality
16	Common	Common

* Inputs 3 – 6 and outputs 7-10 are differential pairs.

- **PWM Signals**: High-side and low-side PWM are RS-422 compatible differential inputs. The termination impedance of the differential receiver is 120 Ω. Overlap protection is implemented through the UCC21710 gate driver IN+ and IN- pins to prevent both the high-side and low-side gates from turning on simultaneously. The overlap protection should not be used as a dead time generator.

- **/FAULT Signals**: The /FAULT signal is a RS-422 compatible differential output with a maximum drive strength of 20mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. The /FAULT signal is a generated on the board by performing an AND operation of the /FLT and RDY pins of the gate driver. The /FLT signal indicates an overcurrent fault while the RDY indicates power-ready.

  LEDs on the board indicate /FLT and RDY signals before the AND operation (DTI = /FLT_LS, DT2 = /FLT_HS, DT3= RDY_LS, DT4 = RDY_HS). In the no-fault state, the RDY LEDs (green) will be on, and the /FLT LEDs (red) will be off.

- **RTD (NTC):** RTD output is a differential signal that returns the resistance of the temperature sensor (NTC) if available. The signal is a duty cycle modulated signal that encodes the resistance of the temperature sensor. The approximate temperature of the module can be determined from this resistance.

- **Reset-Input:** This is a single-ended input that is buffered and passed-through to the gate driver. Refer to the UCC21710 gate driver datasheet available from TI for RST/EN functionality.

7. Board Description

Power Supplies:

Two isolated DC/DC converters (R12P21503D (+15V/-3V) are installed on the board for generating the gate drive bias supplies. Alternatively, the installed DC/DC converter may be replaced by the part numbers below.

1. MGJ2D121505SC for +15V/-4V gate drive bias
2. MGJ2D122005SC for +20V/-5V or +18V/-5V gate drive bias
3. R12P215S +15V single output for unipolar gate drive. If unipolar gate drive is desired, a 0-ohm resistor or shorting wire must be placed between the Source and VSS rails on both the high-side and low-side. On the low-side, short out CB12 and CB13. On the high-side, short out CB8 and CB9. This is shown in Figure 2 below.

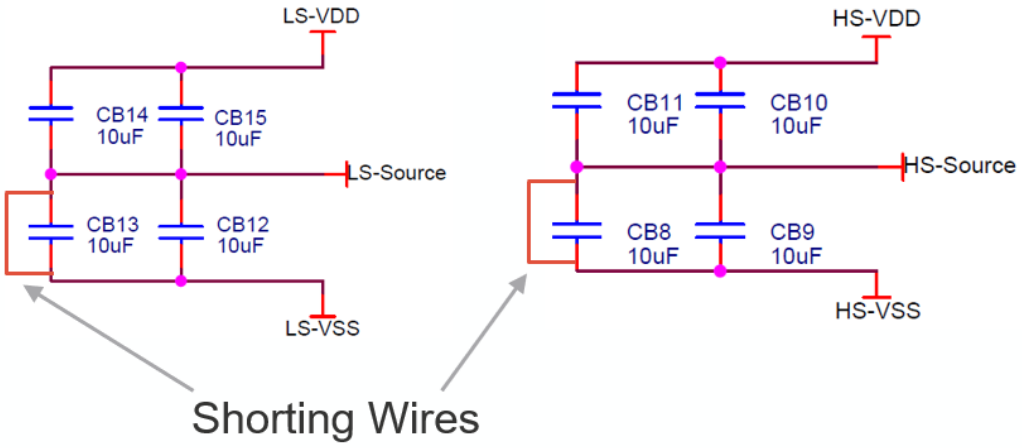

Figure 2. Unipolar drive configuration

Additionally, a 5V supply is generated on the board using a simple 1A LDO with a +/-4% accuracy. This 5V supply is used to power the low voltage side of the UCC21710 gate driver, the differential driver and other logic components on the board.

Gate Resistance

The user may adjust the switching characteristics by adjusting the value of the gate resistor's R27, R28, R30, R31. The default installed gate resistor for both the turn on and the turnoff path is a SMD 1 OHM 1% 1.5W 2512 resistor.

Reverse Polarity Protection

The VIN pin is protected from reverse polarity by a diode and MOSFET in-line with the input to protect against connecting a power source with positive and negative polarity reversed.

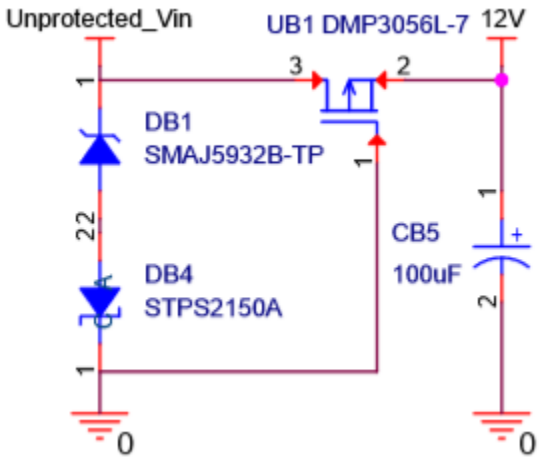

Figure 3. Reverse polarity circuit

Over-Current Fault

The UCC21710 gate driver over-current protection based on a desaturation circuit is implemented on this board. An overcurrent fault is an indication of an over-current event in the SiC MOSFET or power module. The over- current protection circuit measures the drain-source voltage, and the fault will indicate if this

voltage has risen above a level corresponding to the safe current limit. When a fault has occurred the corresponding gate driver channel will be disabled, and the gate will be pulled down. The FAULT-OUT* pins indicate the fault detection. The device is latched unless reset signal is received from the Reset-Input pin. The latching fault only disables the output of the device that detected the fault. The other device may continue to operate based on the PWM inputs.

The OC pin on the driver has a 0.7V threshold with respect to the source of the MOSFET. The detection level is set to ~7V on the board but can be re-calculated. Refer to the UCC21710 datasheet available from TI for re-calculation details.

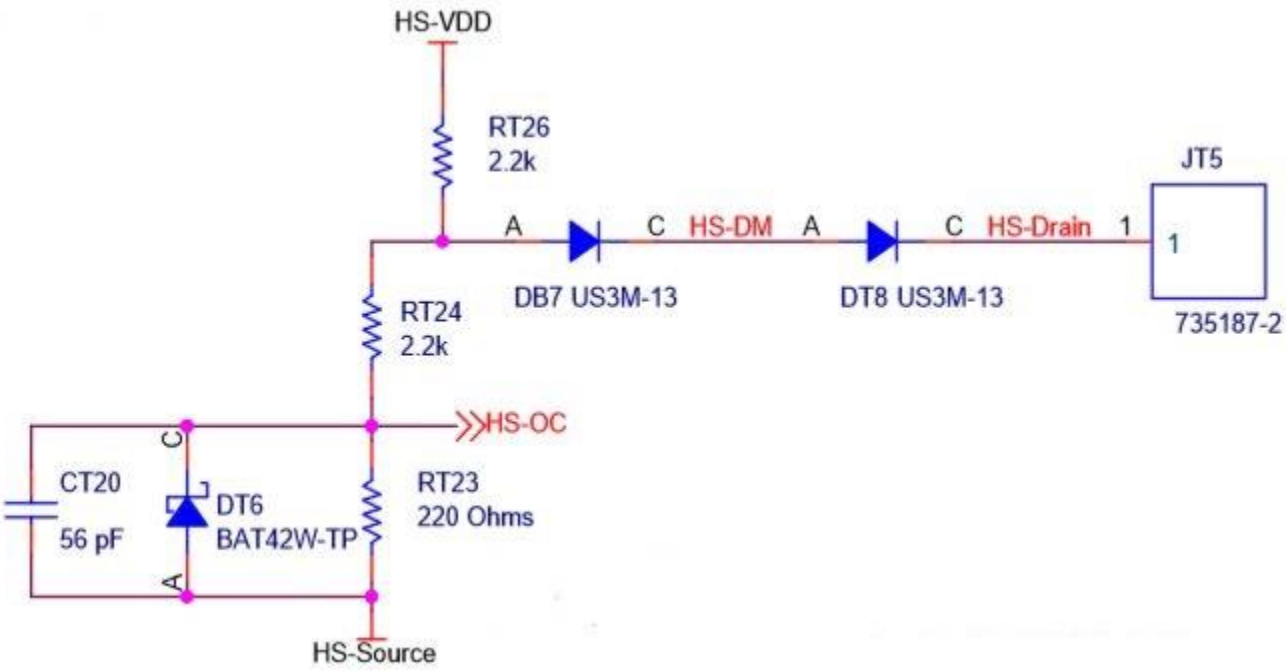

Figure 4. Overcurrent detection circuit

Under-Voltage Protection:

Undervoltage of the output rails of the isolated DC/DC converter and the 5V VCC supply (generated by an LDO on board) are monitored by the UCC21710 gate driver. The gate for the channel where the fault occurred will be pulled low for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. Information on the tolerance and hysteresis can be found in the datasheet for the gate driver available from TI.

Temperature Sensing:

A Negative Temperature Coefficient (NTC) resistor can be read by utilizing the isolated analog (AIN) to PWM (APWM) signal function on the UCC21710 gate driver. The duty cycle of a 400Khz PWM is observed on RTD-Output* which increases linearly from 10% to 88% as the NTC1 voltage decreases from 4.5 V to 0.6 V.

8. Signal Chain Block Diagram

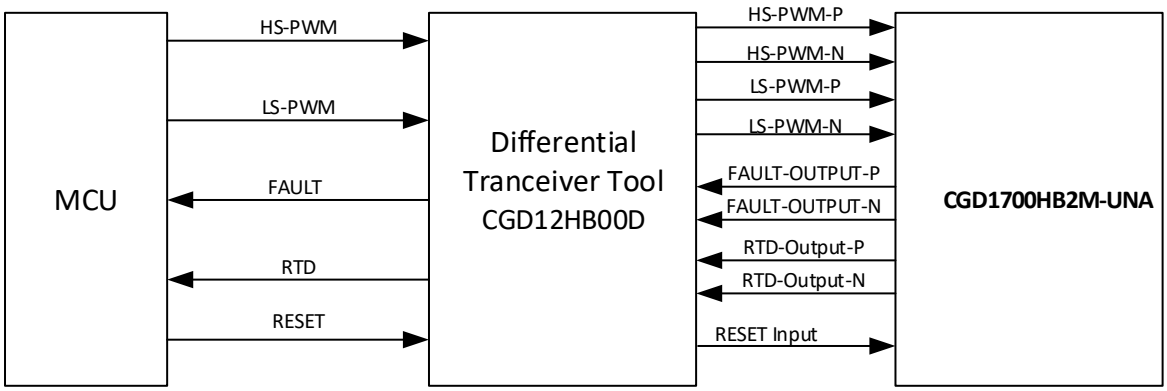

Figure 5. Signal Chain Block Diagram

9. Driver Interface

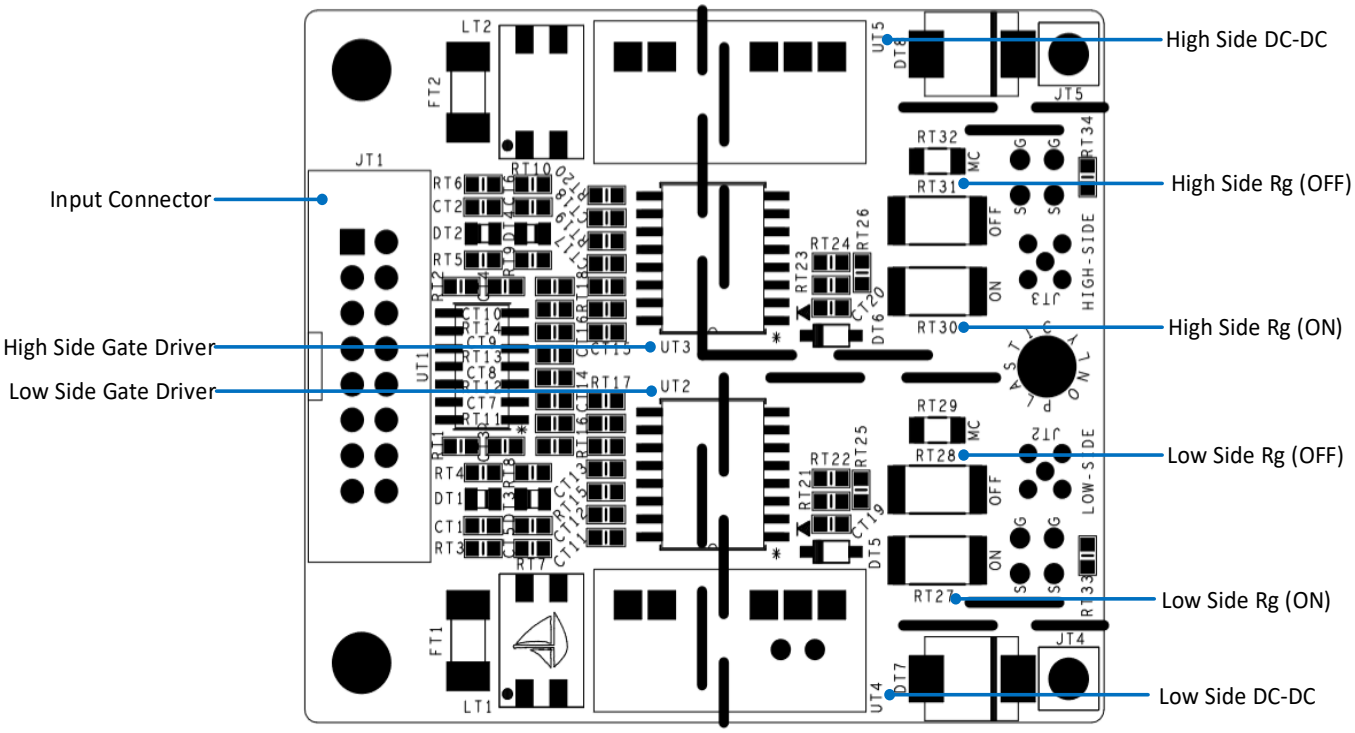

Figure 6. Top View

10. Power Estimates

The gate driver power required is calculated using the formula below. The gate charge is dependent on the datasheets of the MOSFET's or module being driven. Once the required gate driver power is calculated, the required input power can be calculated from the efficiency curves on the power supplies datasheet. This calculation is for one channel of the gate driver.

$$P_{sw} = Q_G * F_{SW} * \Delta V_{PS}$$

P_{sw}: gate driver power (per channel)
Q_G: total gate charge (MOSFET gate charge × number of MOSFETs per switch position)
F_{SW}: switching frequency ΔVPS: difference in isolated power supply voltage rails ($V_{PS,HIGH}$ - $V_{PS,LOW}$)

Example: Calculate the maximum switching frequency for a MOSFET or module with Q_G=1330 nC.
$V_{PS,HIGH}$= 15 V (isolated power supply's positive output voltage)
$V_{PS,LOW}$ = -5 V (isolated power supply's negative output voltage)
ΔV_{PS} = 20 V

2W = 1330 nC* F_{SW} * 20 V
$F_{SW\text{-}Max}$ ≈ 70 kHz with margin

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11. Revision History

Revision	Date	Notes
1	2021-01	Initial Release

12. Important Notes

- This product is meant to be used as an evaluation tool in a lab setting and to be handled and operated by highly qualified technicians or engineers. The product is not designed to meet any particular safety standards and the tool is not a production qualified assembly.
- This board, including any part that is used in this board and is manufactured by an entity other than Cree or one of Cree's affiliates, is provided "as is" without warranty of any kind, including but not limited to any warranty of non-infringement, merchantability, or fitness for a particular purpose, whether express or implied. There is no representation that the operation of this board or each such part will be uninterrupted or error free.
- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.
- The SiC MOSFET that will be used in conjunction with this board switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and reduce the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.