Accuracy Evaluation and Proposed Dynamic Tuning Procedure of a Compact SiC SPICE Model

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Abstract

The commercialization of wide bandgap technology has increased demand for accurate circuit-level simulation models of devices such as Silicon-Carbide (SiC) MOSFET power modules. These models assist with design challenges such as minimizing overshoot and electromagnetic interference associated with wide bandgap switching speeds. However, it is challenging to create highly accurate models across all the conditions that the device may be operated in, such as varying gate resistance, temperature, operating voltage, and operating current. A major contributor to this problem is that the procedure for characterizing and modeling SiC MOSFETs is simplistic relative to their complexity in switching. In particular, the standard methods for characterizing and modeling the device capacitances are simplified, ignoring dependencies on voltage biases and frequency. However, increasing the model complexity to address these issues is generally not feasible because 1) the models must be efficient to converge and simulate quickly, and 2) the necessary characteristics are often impossible to measure. Rather than increasing the model complexity, this paper builds upon a previously presented compact behavioral model and applies a dynamic tuning procedure to improve alignment with empirically derived datasheet parameters. The procedure is applied to a half-bridge SiC MOSFET power module model and it is demonstrated that the overall dynamic accuracy of the model is increased by 50% across a wide range of double pulse test conditions. While this procedure further divorces the behavior model from physical reality, the tradeoff is acceptable given the purpose of this model: accurately predicting device behavior in application while minimizing computational complexity.

1 Introduction

Improvements to wide bandgap (WBG) semiconductors, such as Silicon-Carbide (SiC) MOSFETs, have increased the efficiency and power density of converter applications [1]. Multi-chip power modules (MCPMs) further these performance advantages by offering easy-to-implement packages that are optimized for their high edge rates and power levels. The performance advantages are enabling growth in new technologies, such as long-range electric vehicles [2]. Furthermore, despite higher up-front cost for the semiconductors, the reduction in the necessary passive components often yields an overall reduction in cost.

In order to take full advantage of the capabilities of WBG power devices, designers must optimize their system layout to mitigate the drawbacks of fast edge rates. Typically, this requires improving packaging, passive components, and system layout, which incurs additional development costs and presents new challenges for designers unfamiliar with WBG power electronics [2]. Simulation tools offer a method to reduce time and cost through virtual prototyping studies that inform hardware decisions or facilitate optimization. Compact behavioral models implemented in circuit-level solvers (such as SPICE) are particularly useful for optimization as they can predict the system behavior at specified conditions and can evaluate shifts in behavior caused by parasitic elements.

The SPICE models necessary for these simulations are usually provided by device manufacturers. These models are generated by measuring the “static” characteristics of the device and fitting parameters in equations to the measured data. Here, “static” refer to characteristics that are obtained during quasi-steady-state operation, such as the conduction characteristics, small-signal device capacitances, gate resistance, and parasitic elements. The models fit to these input characteristics are then used to predict how the device behaves when switched in a full system. However, this presents some fundamental issues with the approach. First, it assumes that these device characteristics are adequate for predicting switching,

but the behavior of a MOSFET during switching is much more complex than what is observed during quasi-steady-state measurements. Second, the input dataset is substantially smaller than the number of conditions that the model may be evaluated in. It is unreasonable to expect that a model generated with static characteristics will accurately predict device behavior when switched at any arbitrary set of conditions.

These issues compound with the fact that the provided models must simultaneously have good convergence behavior, be computationally efficient, and accurately predict the device behavior in general circuits. However, this creates a tradeoff: increasing the accuracy requires a more complex model, but in turn a more complex model reduces the efficiency. More complex models also require larger input datasets, increasing the amount of testing required per part. Thus, the implementation of these models must be simple to ensure that they are able to be created and simulated.

Because it is unrealistic to develop a general model that can accurately predict switching for any arbitrary condition for all devices, another approach is to use the switching characteristics to tune the parameters of the device model. This paper presents such a dynamic tuning method that can improve its accuracy without increasing its complexity. The dynamic tuning procedure is applied to a CAB016M12FM3 half-bridge SiC MCPM (shown in Fig. 1) and demonstrates how the accuracy and utility of a model can be significantly improved by applying the approach without increasing the model complexity.

2 Target Model Overview

When selecting a SPICE model for dynamic tuning, it is important to consider the implementation of the SiC MOSFET. In general, MOSFET die-level models can be separated into three distinct categories: physics, semi-physics, and behavioral. Physics-based MOSFET models leverage the fundamental physical parameters of a device to predict its behavior and are generally the most complex [3], [4]. Semi-physics models also leverage device physics equations, but adjustments to the equations are made to improve performance at the cost of physical accuracy [5], [6]. Behavioral models are distinct from physics-based models in that they are decoupled from the physics of the device and can therefore be optimized for simplicity, computational efficiency, or accuracy [7], [8]. Behavioral models follow a “black-box” approach, where the implementation is arbitrary with intent only to provide the desired output. For dynamic tuning, this arbitrary design of behavioral models provides

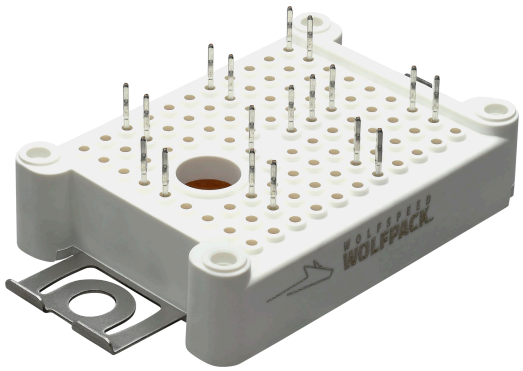

Fig. 1 Test subject for dynamic tuning procedure - CAB016M12FM3 power module

an advantage because the equations and parameters can be adjusted freely to improve the accuracy of the output. In addition, equations and parameters within behavioral models are usually specific to one aspect of behavior, and thus can be adjusted without affecting other model behaviors.

This paper applies the dynamic tuning approach to a previously presented robust and efficient behavioral compact SiC MCPM SPICE model [9]. The general architecture of the module model is shown in Fig. 2. The model is segmented into a package and die model. The package model connects the die to the module terminals and includes parasitic and thermal elements. The die model includes the electrical characteristics of the MOSFETs themselves. A brief description of the behavior and capabilities of the model is provided in Table 1 and is described in more detail below.

The forward conduction parameters are implemented in a lookup table with dependence on V_{GS}. An $R_{DS(ON)}$ and V_{GS} shift is used to model the temperature dependence. The equations and tables implemented provide excellent agreement with empirical data. The equations also include parameters for fitting the short-channel effects at high-voltage and high-current. These parameters are fit using empirically measured high-voltage high-current static characteristics [10]. This model can accurately predict conduction losses during normal operation and during short-circuit or surge events.

The conduction behavior between first and third quadrant is continuous through the origin, improving convergence and speed. The reverse conduction parameters are also implemented using a lookup table with V_{GS} dependence, and temperature dependence is achieved with a resistance and V_{GS} shift.

The device capacitances are implemented using behavioral current sources, with the capacitance

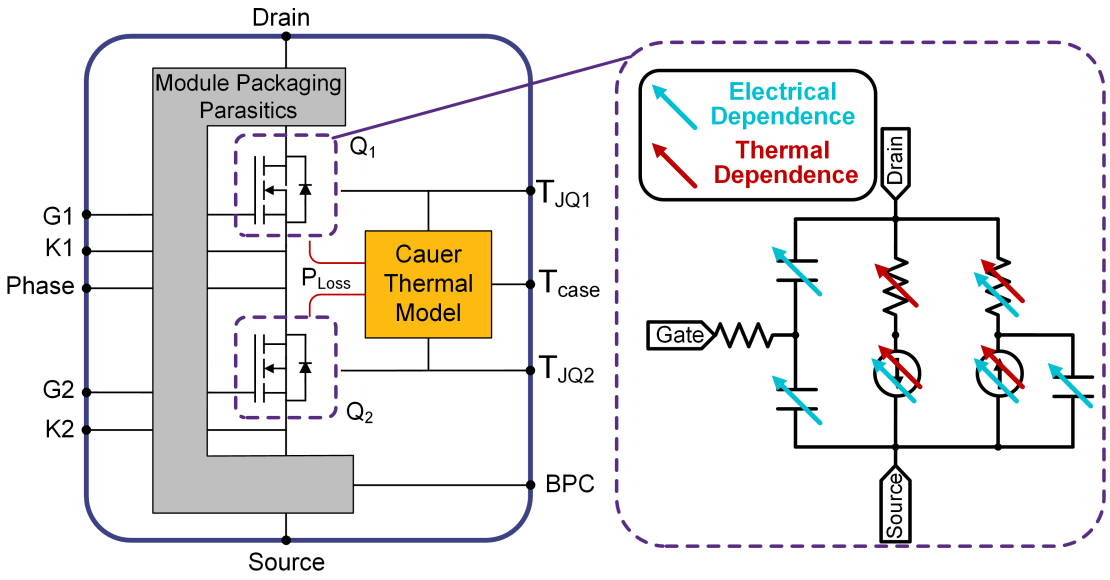

Fig. 2 Half-bridge power module model architecture [3]

at a given voltage bias provided by a lookup table. The capacitance across drain-to-source (C_{DS}) is dependent on the drain-source voltage (V_{DS}), the capacitance across gate-to-drain (C_{GD}) is dependent on across gate-drain voltage (V_{GD}), and the capacitance across gate-to-source is dependent on the gate-source voltage (V_{GS}). This method is simple to quantify, implement, and is efficient to simulate.

Behavior	Model Implementation
Forward Conduction	Full dependence on V_{GS} (0 V – 18 V) and T_J (25ºC – 175ºC). V_{DS} biases include up to the bus voltage.
Reverse Conduction	Full dependence on V_{GS} (-5 V – 18V) and T_J (25ºC – 175ºC).
Device Capacitances	C_{GD} dependence on V_{GD}, C_{DS} dependence on V_{DS}, C_{GS} dependence on V_{GS}
Reverse Recovery	Modified lumped-charge reverse recovery model with dependence across temperature, derived from [12] and [13].
Parasitic Network	Per-terminal power terminal inductance, gate loop inductance, per-terminal baseplate capacitances.
Thermal Network	Closed-loop electrothermal behavior with a 3rd-order Cauer network.

Table 1 Brief description of leveraged model behaviour based on work in [3]

The reverse recovery model is based on a lumped-charge model first presented in [11] and modernized in [12]. The parameters are implemented in a lookup table with dependence on temperature. The reverse recovery parameters are decoupled from the reverse conduction parameters such that they can be tuned independently. This allows for the model to predict changes in reverse recovery charge, losses, and current overshoot across temperature.

The parasitic model includes the partial inductance from each terminal to the die (both power and gate), along with the baseplate capacitance for electromagnetic emission simulations. A 3rd-order Cauer network is included to model temperature changes in the die caused by power losses and heat exchange with the baseplate.

2.1 Determining Model Accuracy

The accuracy of a SPICE model depends on the conditions in which it is being evaluated in simulation. SPICE models can be used to predict various behaviors (i.e. conduction losses, short-circuit survivability, voltage overshoot, switching losses, and reverse recovery losses), and the accuracy of that prediction also depends on the conditions specified in the circuit. In general, the conduction losses are well predicted by the model of the forward and

reverse static characteristics. However, the switching characteristics are more complex and more difficult to accurately predict. The transient behavior is also often an important consideration for designers implementing these devices into their systems. For these reasons, the focus in this work is on improving the accuracy of the transient characteristics, such as slew rates, switching losses, and reverse recovery.

There are two common methods for validating the transient characteristics of SPICE models. The first method, known as qualitative model analysis, uses overlain waveforms to observe agreement between the simulation and empirical data. Several models in the literature apply this approach to validate their models at a small number of operating conditions [13], [14]. However, this method has several disadvantages. First, it is a subjective metric that cannot be consistently applied across tests and models. Second, the model accuracy is sensitive to the operating conditions of the circuit; a model that is accurate at one operating condition will not necessarily be accurate at another. It is important to vary the operating conditions include the gate resistance (R_G), temperature (Tj), operating voltage (V_{bus}), and operating current (I_{load}). Because of the number of parameters that can be varied, the test matrix is often very large, and it is unreasonable to apply the method across many tests.

An alternative method, quantitative model analysis, uses a set of clearly defined metrics to quantify the transient characteristics of a DPT waveform. Each parameter is given a specific definition such that it can be calculated consistently through automated means across various operating conditions for both simulation and experimental data. This technique has been applied in the literature, but the number of operating conditions considered are often limited [15], [16], [17].

The quantitative metrics chosen for this analysis are described in Fig. 3. The selected parameters encompass only a small subset of the overall device behavior but describe important features of switching dynamics. In Fig. 3 (a), the V_{DS} and I_{DS} waveforms at turn-off and turn-on are parsed to obtain the slew rates for each transition. In this work, the slew rates are calculated at the average slope between 10% and 90% of the nominal operating point. For example, dv/dt(off) would for a DPT at a bus voltage of 600 V would be calculated between 60 V - 540 V. In Fig. 3 (b), the instantaneous power waveforms are integrated to obtain the switching energies, E_{off} and E_{on}. The switching energies are integrated between 10% V_{DS} and 10% I_{DS}.

Any waveform metric that can be programmatically calculated on a waveform can be considered. Some examples include the reverse recovery energy, peak reverse recovery current, and the turn-

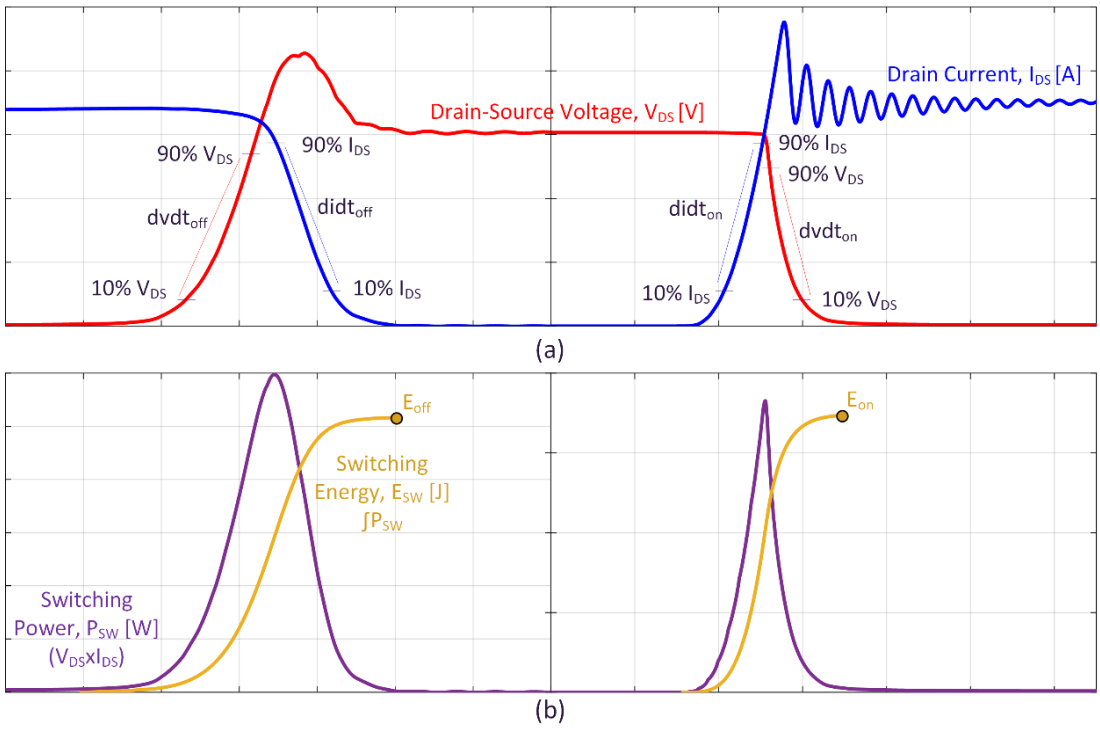

Fig. 3 Description of quantitative model metrics, (a) V_{DS} and I_{DS} waveforms for slew rate calculation, and (b) instantaneous power and integrated energy waveforms for SW energy calculations

off and turn-on delay. These metrics should be selected based on which characteristics are important for the model application.

With the quantitative metrics selected, the method for determining model accuracy is as follows. First, a model of the CIL test circuit is implemented in a SPICE solver software. Second, the simulation is run at a set of conditions that match the empirical data. Third, both the empirical data and the simulation waveforms are analyzed to obtain the quantified values for each metric. Finally, this information is used to generate an error for each metric that is a function of the operating conditions. These error functions can be used to generate heat maps or histograms to visually understand the error or can be combined to generate a total sum of error that can be input into fitting functions.

3 Dynamic Tuning Procedure

The procedure for the dynamic tuning approach is outlined in Fig. 4. For the process described here, MATLAB is used to control, quantify, and tune while and LTspice was selected for model simulation, but any high-level language and SPICE solver could be used.

First, a set of DPT conditions appropriate for the device are selected. The conditions should vary across R_G, T_J, V_{bus}, and I_{load} within the recommended bounds of operation for the part. However, while many tests can be used for accuracy validation, the number of tests used for fitting should be limited to 10-20 conditions. If too many conditions are selected, the required time for tuning will become excessive because the solver must simulate the circuit at all conditions for each iteration.

Second, MATLAB calls LTspice to run the simulation at each specified condition. The LTspice waveforms are processed to obtain the quantitative metrics from Fig. 3. The error for a single DPT operating condition is calculated by equation (1), where *emp* is the quantitative metric value for empirical data and *sim* is the quantitative metric value for simulation data. The error for each metric is summed to obtain the total error for a specific DPT condition. Finally, the total error for each DPT condition is summed to obtain a total error between the simulation and the model. This process can be changed as necessary, such as by applying weights to specific conditions or tests or by using other methods to sum the errors. It is only necessary that the result is a single error value that can be input to a fitting function.

$$Error = abs\left(\frac{emp - sim}{emp}\right) \quad (1)$$

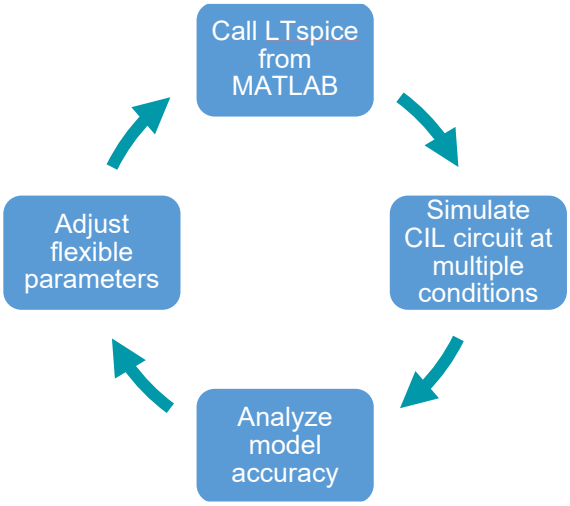

Fig. 4 Dynamic tuning process

Finally, the error term is input into a fitting function that adjusts the model parameters to decrease the error, and the cycle repeats until a certain number of iterations or tolerance is reached. The fit function will balance the adjustment of parameters to minimize the error across all of the provided conditions, resulting in a robust and balanced model that is useful and accurate across the various conditions the model may be used in.

3.1 Selecting Flexible Tuning Parameters

The model parameters that are adjusted by the fitting function should meet a set of criteria. First, the transient behavior should be sensitive to changes in the parameter value; otherwise, the tuning algorithm may change the parameter arbitrarily and cause unintended effects. Second, changing the parameter to improve transient behavior should minimally affect other behaviors of the model. For example, if a parameter affects the on-state resistance, changes to it may increase conduction loss error. Finally, it should be reasonable to change the parameter within certain bounds. If a parameter has a well-defined and strict definition, then it is not suitable for tuning. For example, the commutation inductance of a module package can be well-defined by impedance analysis measurements. Significantly adjusting this parameter in the model can make it non-physical.

Considering the above criteria, the most flexible parameters for tuning are those related the device capacitances of the SiC MOSFET and the internal gate resistance: C_{DS}, C_{GS}, C_{GD}, and R_{GI}. These parameters do not affect conduction losses and primary purpose in a model is to control the transient behavior. Most importantly, the standard measure-

ment and modeling procedures for these characteristics are oversimplified. They are generally represented as having a single voltage dependence in datasheets and device models. However, it has been shown repeatedly that the device capacitances are highly dependent on both V_{DS} and V_{GS} biases [18], [19], [20], [21], [22]. There is also evidence that they are sensitive to the stimulus frequency at which capacitances are measured [10]. Quantifying a simultaneous V_{DS} and V_{GS} bias is challenging because applying DC current will flow through the device while V_{GS} is above the threshold voltage, leading to device failure. Attempts to solve this issue have been made, such as using a custom pulsed setup that applies a pulsed V_{GS} and V_{DS} bias and performs a small-signal measurement of the capacitances within this window [22] or leveraging physics-based simulation software [20]. Implementing these processes to characterize and model the physical device capacitance behavior is unrealistic for creating SPICE models. Instead, the dynamic tuning procedure described herein can adjust the simplified device capacitance model to match the transient behavior without increasing model complexity.

The internal gate resistance is similar to the device capacitances and has additional complexity that is ignored in modeling. While this parameter is modeled as a lumped resistance, it is actually a distributed resistance that is both frequency and temperature dependent. The transient behavior is also highly sensitive to the internal gate resistance making it suitable for tuning.

The selected tuning parameters and their descriptions are provided in Table 2. The gate-drain capacitance is multiplied by A_{GD} and has an added offset O_{GD}, as shown in equation (2). The C_{GD} term is V_{GD}-dependent, and the scaling terms are applied equally at all biases. O_{GD} can be negative, but is bounded such that $C_{GD,effective}$ is not negative. The gate-source capacitance is scaled by A_{GS} but does not include an added offset, as shown in (3). This is because, while C_{GS} is a largely constant term, the C_{GD} capacitance decreases by several orders of magnitude from low V_{GD} to high V_{GD}. As such, O_{GD} has a larger effect at high V_{GD}, while A_{GD} has a larger effect at low V_{GD}, yielding more tuning control. Finally, the internal gate resistance is scaled by A_{RGI}, as shown in equation (4). Scaling of C_{DS} is omitted because it can cause errors with overpredicting reverse recovery and Q_{OSS} losses.

$$C_{GD,effective} = A_{GD} * (C_{GD}(V_{GD}) + O_{GD}) \quad (2)$$

$$C_{GS,effective} = A_{GS} * C_{GS}(V_{GS}) \quad (3)$$

$$R_{GI,effective} = A_{RGI} * R_{GI} \quad (4)$$

Parameter	Description
A_{GS}	Scalar multiplier to gate-source capacitance equation
A_{GD}	Scalar multiplier to gate-drain capacitance equation
O_{GD}	Added offset to gate-drain capacitance equation
A_{RGI}	Scalar multiplier to internal gate resistance

Table 2 Description of parameters selected for dynamic tuning

3.2 Dynamic Tuning Results

To demonstrate its effectiveness, dynamic tuning procedure was applied to a CAB016M12FM3 power module SPICE model using the metrics described in Fig. 3 and tuning the parameters described in Table 2. For the initial conditions, the scalar parameters were set to 1 and the offset parameter was set to 0 (meaning that the parameters have no effect on the model). The empirical CIL data was collected on a KIT-CRD-CIL12N-FMA Wolfspeed® evaluation kit shown in Fig. 5. Over 1,000 CIL test conditions were evaluated on this setup. However, for tuning, the smaller subset of conditions shown in Table 3 was considered. The

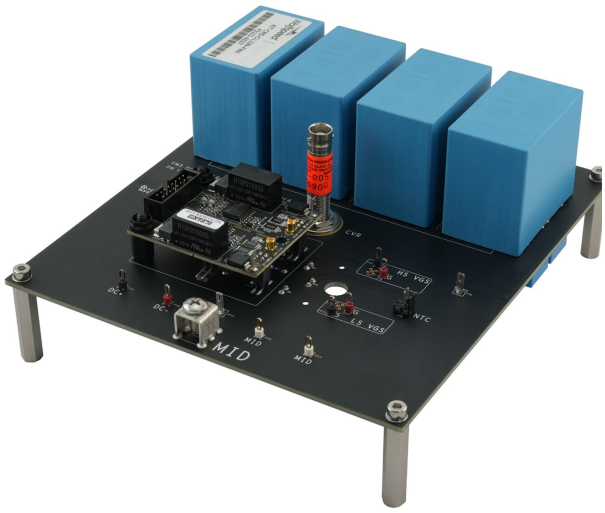

Fig. 5 KIT-CRD-CIL12N-FMA CIL evaluation kit for evaluating CAB016M12FM3 power module

T_J (ºC)	R_G (Ω)	V_{bus} (V)	I_{load} (A)
25	0	800	30
25	0	800	90
25	0	800	150
25	3	800	30
25	3	800	90
25	3	800	150
25	10	800	30
25	10	800	90
25	10	800	150
150	4	800	30
150	4	800	90
150	4	800	150

Table 3 DPT conditions selected for dynamic tuning

selected conditions consider a wide range of gate resistance, load current, and temperature conditions. A single bus voltage is used because most module operation will occur at 800 V. More conditions can be included but doing so increases the tuning time.

As mentioned previously, the error between the simulated DPT and the empirical measurements for each of the quantified metrics in Fig. 3 is calculated for each condition in Table 3 to yield the total model error. The mean error across all conditions for each metric before and after tuning is shown in Fig. 6. For this model, each metric shows a significant reduction in error. For example, the error in $dvdt_{Off}$ decreased from 48.9% to 18.5%, and the error for E_{Off} decreased from 26.4 % to 12.9 %. To achieve this reduction in error, A_{GS} decreased to 0.68, A_{GD} increased to 1.47, O_{GD} increased to 5.8 pF, and A_{RGI} decreased to 0.84.

It should be noted that Fig. 6 represents only a small subset of the overall dataset and potential operating conditions. Thus, an additional heat map that compares the empirical DPT data and SPICE simulation model across a wider set of conditions is provided in Fig. 7. Each subplot shows the error between the empirical data and the simulation model for one of the six parameters defined in Fig. 3. The color of the surface at each X and Y coordinate indicates the error at an R_G and I_{load} condition for V_{bus} = 800 V and T_j = 25ºC. Warm colors indicate more error, and cool colors indicate less error. Before tuning in Fig. 7 (a), the model error is quite high, especially for the turn-on event. The turn-on loss error exceeds 100% in many cases and is no lower than 40%; $dvdt_{On}$ exceeds 50% at

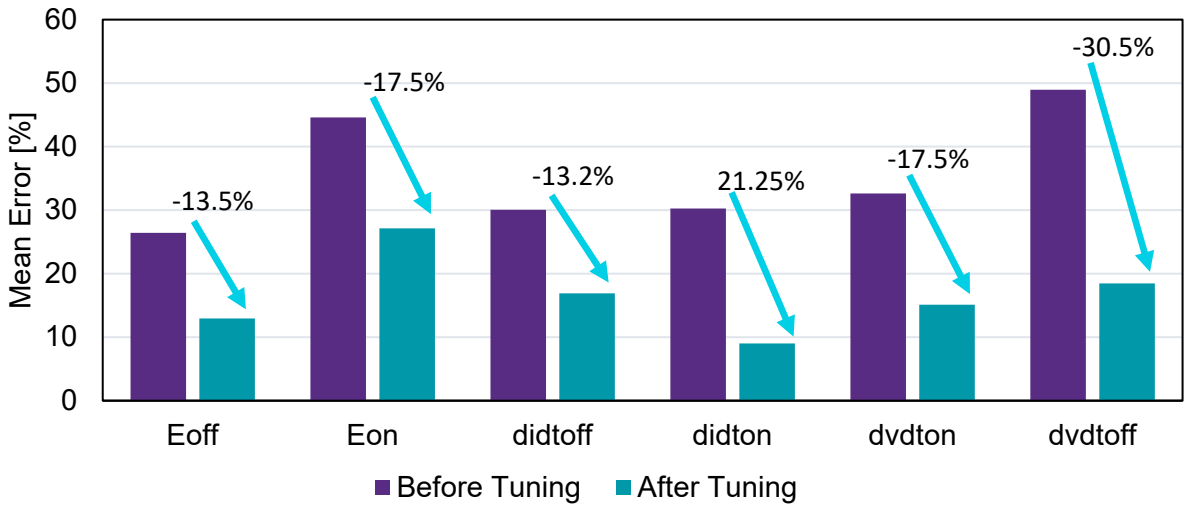

Fig. 6 Reduction of individual error metrics before and after tuning

most conditions, and the $didt_{On}$ is no lower than 40% at any condition.

After applying the dynamic tuning procedure in Fig. 7 (b), the error for each metric improves considerably. The E_{On} error decreases to less than 40% in all conditions, and under 10% error below a 2 Ω gate resistance. The $dvdt_{on}$ error decreased to below 30% at all conditions, and the $didt_{On}$ error decreased from above 40% across all conditions to less than 10%. Overall, the model demonstrates extremely good agreement with the empirical measurements across a wide range of operating conditions after tuning. This improves the overall utility of the model as it and can more accurately predict the slew rates and switching losses.

The improvement in model accuracy can be observed in waveform overlays as well. Fig. 8 shows an overlay between the empirical measurements and simulation results before and after tuning at 800 V, 25ºC, 70 A, and 2 Ω. While the turn-off

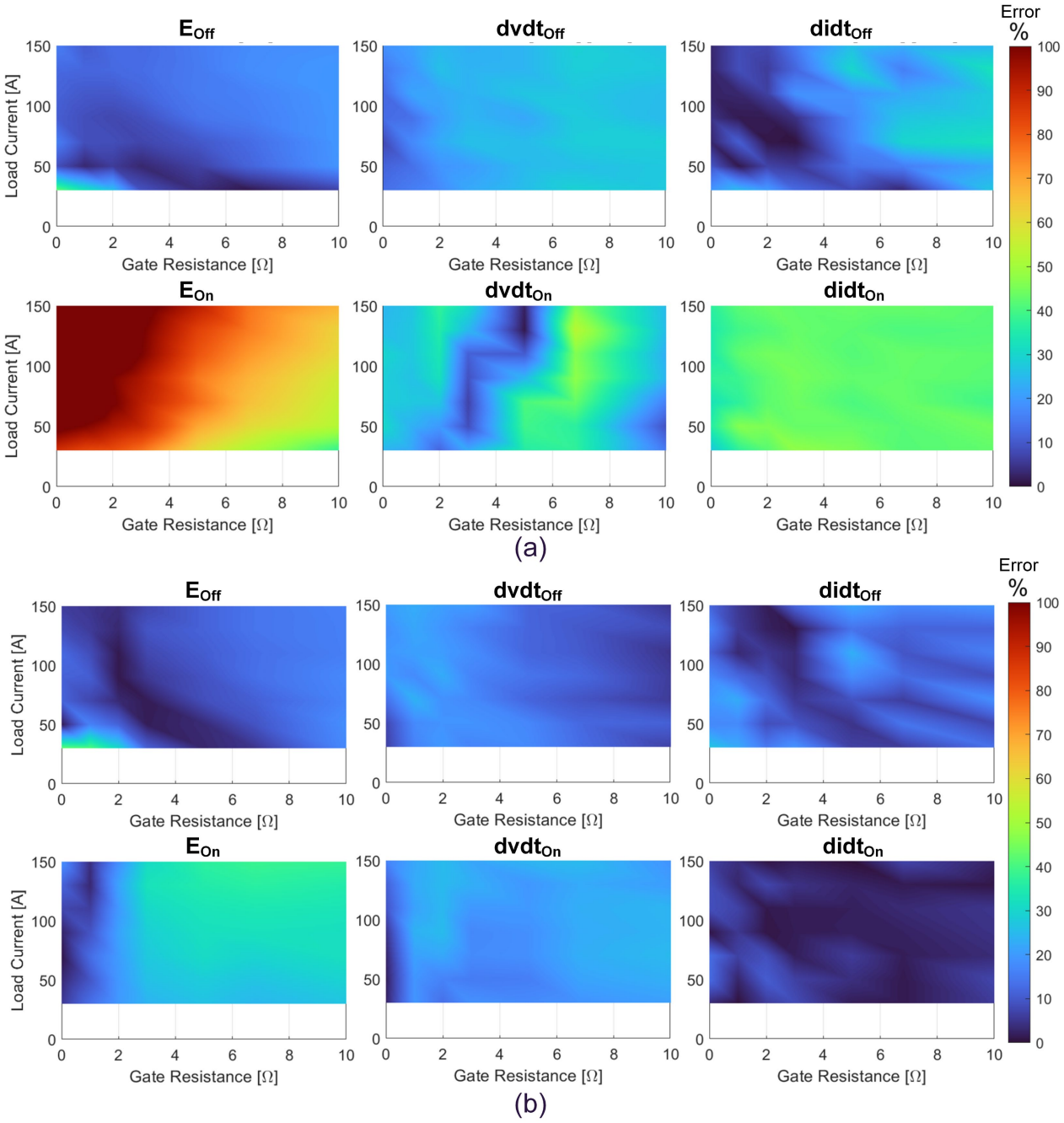

Fig. 7 CAB016M12FM3 model error across gate resistance and load current at 800 V and 25 ºC (a) before dynamic tuning and (b) after dynamic tuning. Subplot titles indicate error parameter. Warmer colors indicate higher error. Color at Y-axis and X-axis coordinate indicate the conditions that the error is observed.

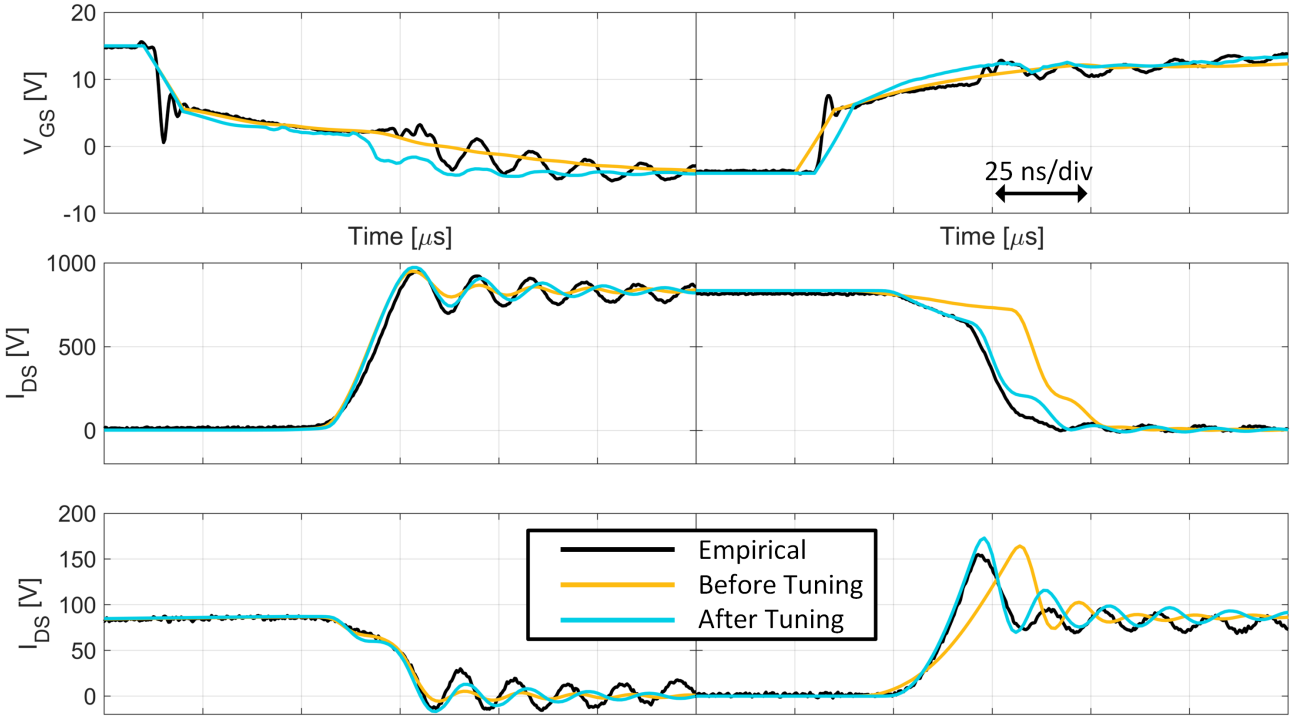

Fig. 8 Turn-off and turn-on DPT waveform overlay comparisons for CAB016M12FM3 SPICE model before and after applying dynamic tuning procedure. DPT conditions are 800 V, 25ºC, 70 A, and 2 Ω.

waveforms are similar between all three, the post-tuning results agree much better with the empirical measurements than before. This demonstrates that not only are the quantified metrics easier to use for a tuning algorithm, but the end results provide good agreement between overlain waveforms as well.

4 Conclusion

Circuit-level simulation models face a distinct challenge in that they are expected to operate efficiently, converge in general circuits of varying complexity, and provide accurate predictions of fast switching edges across a wide range of operating conditions. Developing modelling and characterization techniques that simultaneously satisfy these conditions is extremely challenging and impractical.

Rather than focusing on implementing new model behaviours and developing new measurement techniques, this paper proposes an output-based dynamic tuning approach that uses the measured CIL waveforms of a device to tune its parameters. The final result is a model that more accurately predicts the transient behaviour while retaining its simplicity such that it can operate efficiently in general circuits. This method is easily applicable to device models and provides a general approach to improve transient accuracy without redeveloping the model itself.

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